

Compal Confidential

BAUS0 BAUY0 DIS M/B Schematics Document

AMD Stoney SOC with DDR4

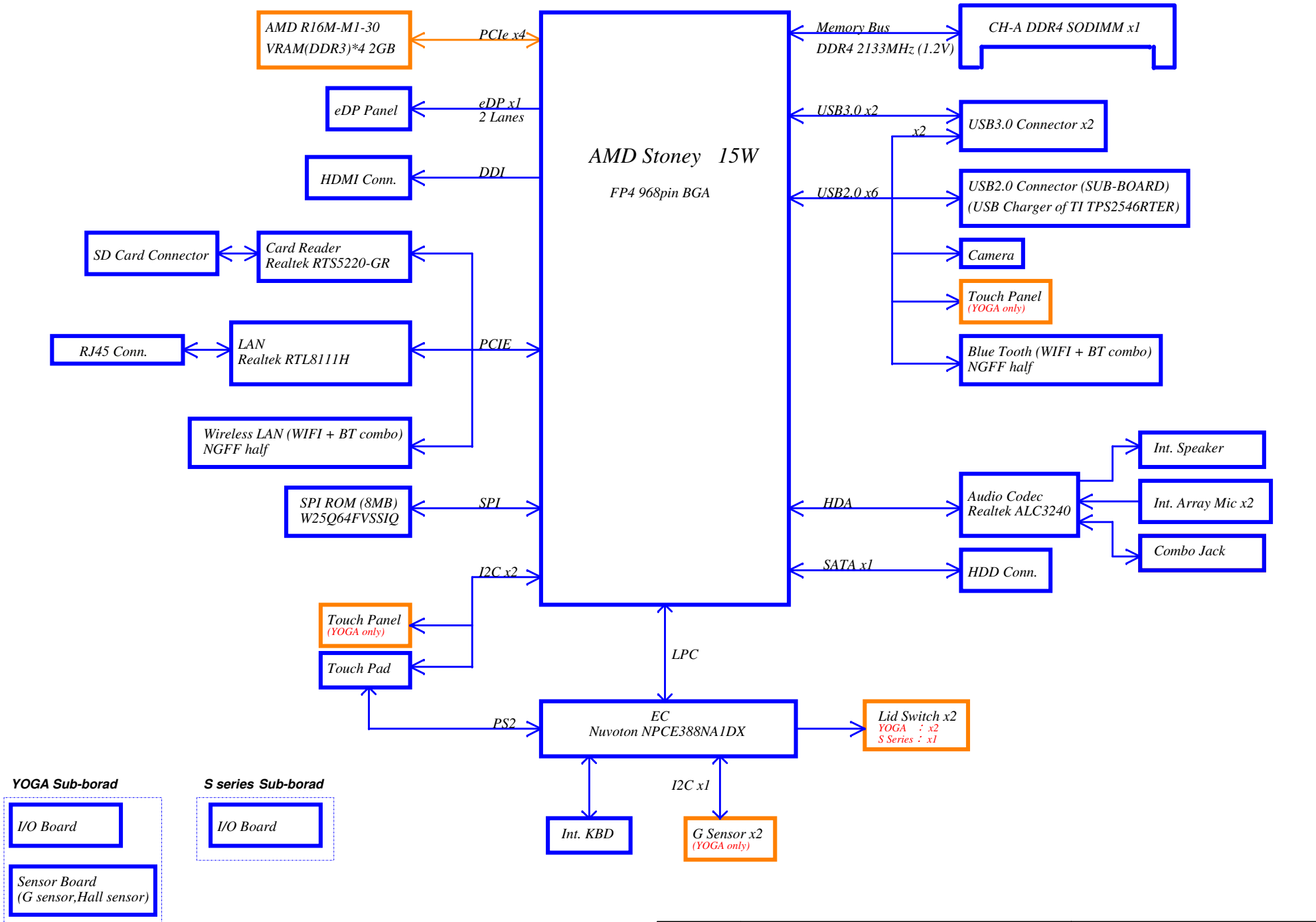
AMD R16M-M1-30

2015-12-17

LA-D541P

REV : 0.2

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Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (20V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V	2.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.5VGS	1.5V switched power rail for VGA	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+0.775VALW*	0.775V always on power rail	OFF*	ON*	ON*

	SOURCE	VGA	BATT	EC	SODIMM	WLAN	Thermal Sensor	APU	CRT RTD2168
EC_SMB_CK1 EC_SMB_DA1	388N +3VALW	X	V +3VALW	V +3VALW	X	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	388N +3VS	V +3VGS	X	V +3VALW	X	X	V +3VGS	V +1.8VS (+3VS)	V +3VS

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
Charger	0001 0010 b	12H	SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

Device	Address	HEX
DDR DIMM1	1010 001Xb	A2H

UAPU1 A9@
SA00009PT00
S IC ZM2901FY23AC 2.9G BGA 968P

UAPU1 A6@
SA00009PU00
S IC ZM2401AVY23AC 2.5G BGA 968P

UAPU1 E2@
SA00009PV00
S IC ZM2001AVY23AC 2.1G BGA 968P

ZZZ
DA6001JJ000
PCB 1NZ LA-D541P REV0 M/B
SS@

ZZZ
DA6001JJ100
PCB 100 LA-D541P REV0 M/B
YOGA@

Port	Device
GPP0	Card Reader
GPP1	LAN
GPP2	WLAN
GPP3	

USB 2.0	USB 3.0	Port	3 External USB Port
		0	USB2.0 (Charger)
		1	Touch Screen
		2	WLAN/BT Combo
		3	Camera
		4	
		5	
		6	USB3.0
XHCI	2	6	USB3.0
	3	7	USB3.0

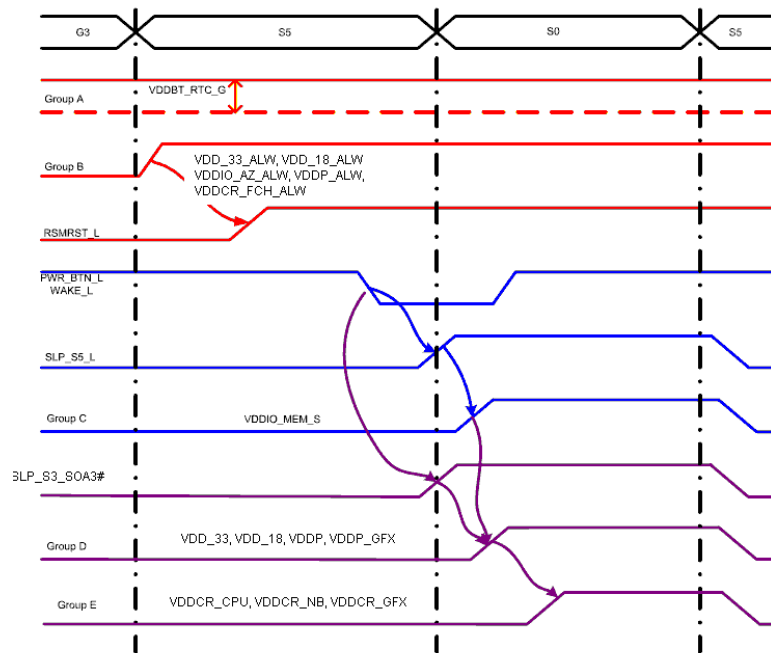
<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALV</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

OC#	USB Port	
0	USB20 port0	
1	USB20 port6,7	USB30 port2,3
2		
3		

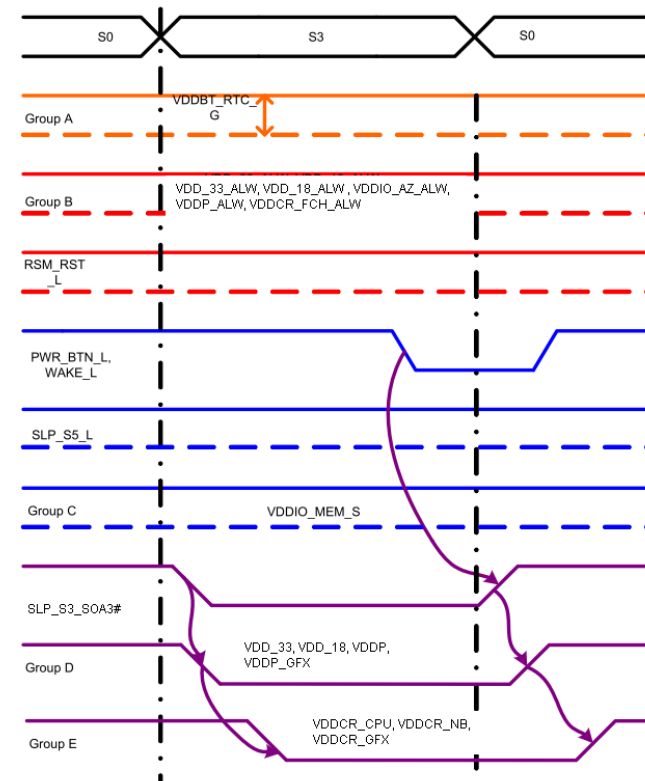
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Power up Sequencing G3 TO S0



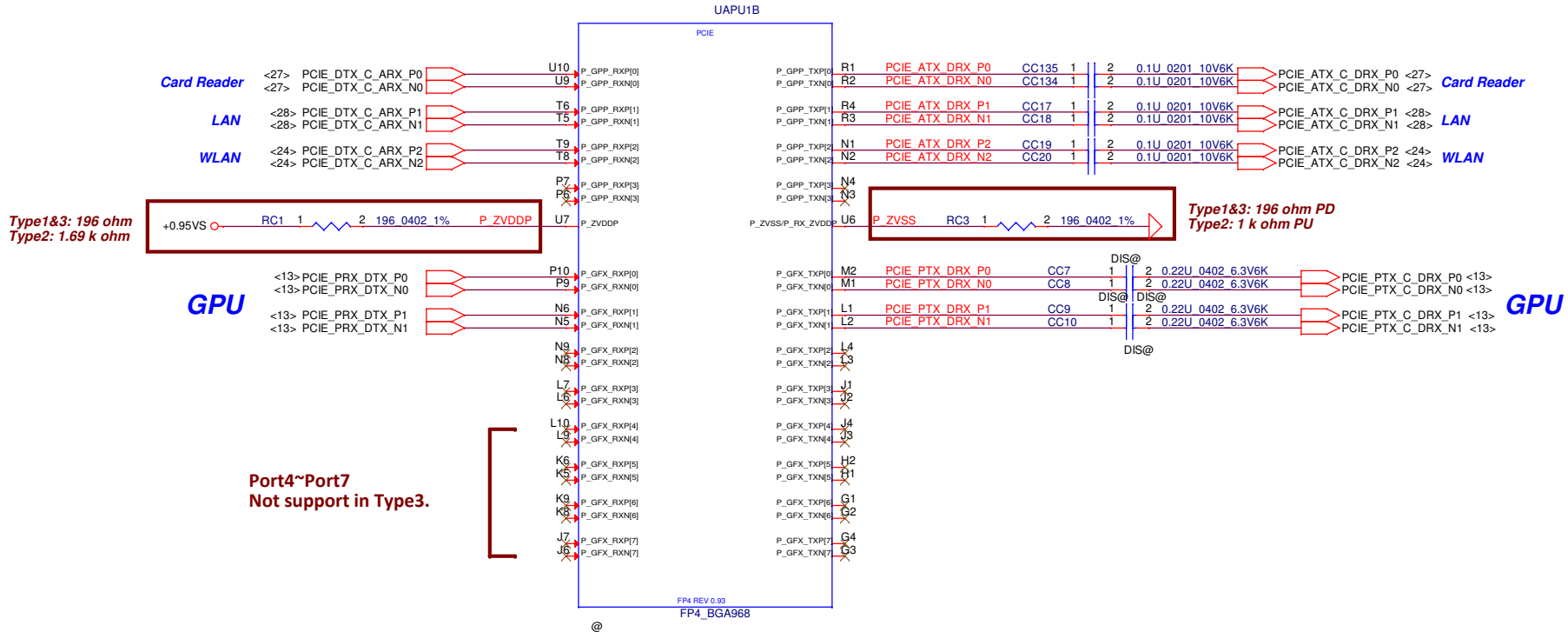
Power up Sequencing S0 TO S3 TO S0



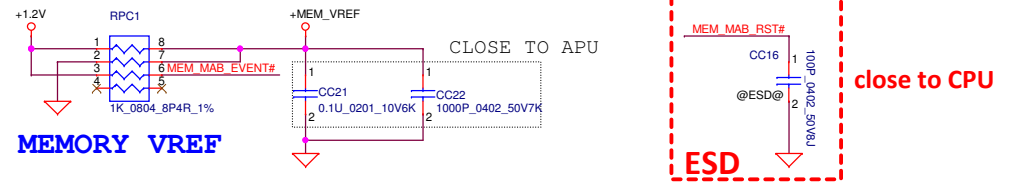
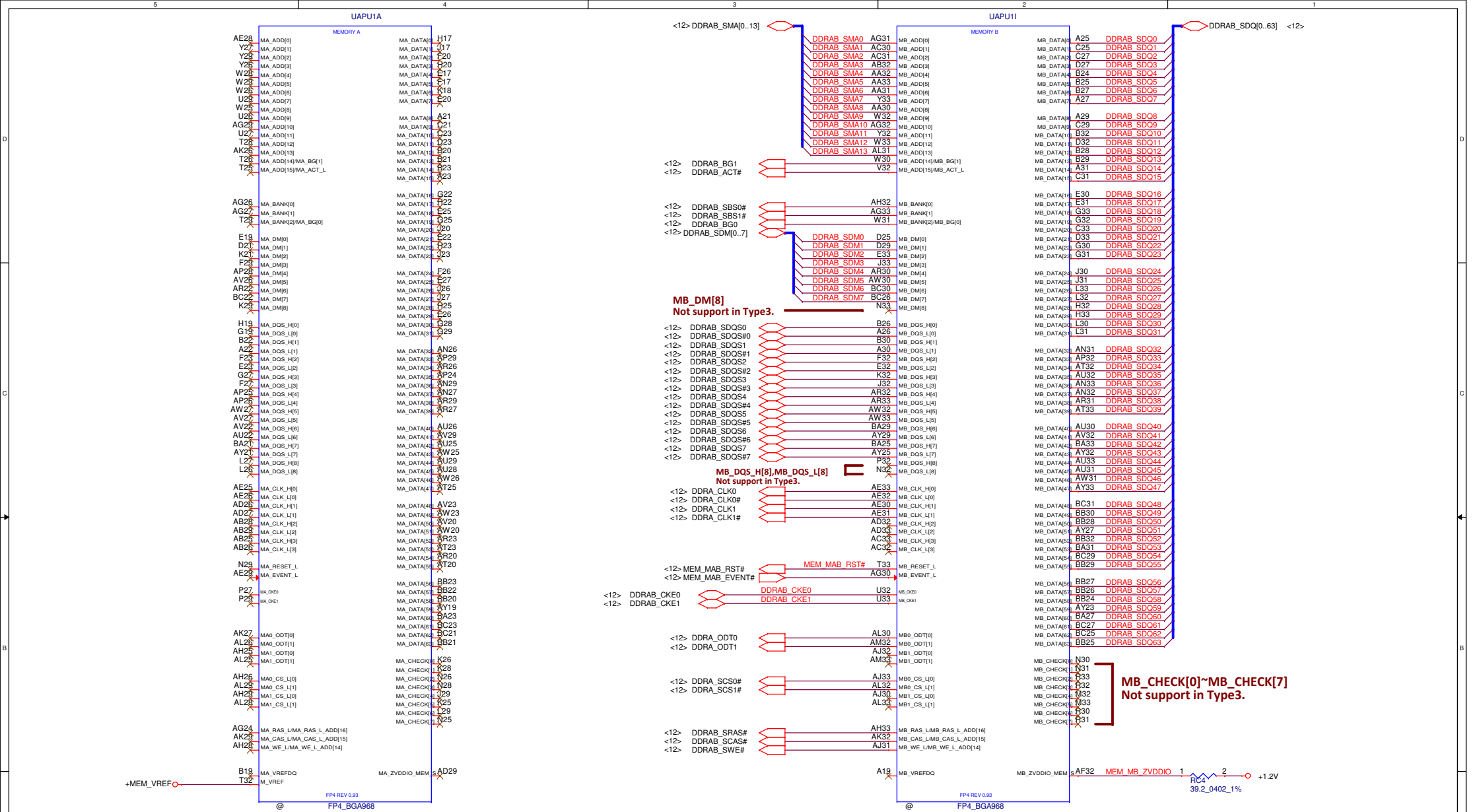
Power on Sequence required:

1. There is no sequencing requirement between power supplies within the individual power groups.
2. All power supplies in Group A must be stable and within specifications for 5 seconds before any power supply in Power sequencing Group B is greater than 10% of its specified minimum operating voltage.
3. All power supplies in Group B must be stable and within specifications before any power supply in Power sequencing Group C is greater than 10% of its specified minimum operating voltage.
4. All power supplies in Group C must be stable and within specifications before any power supply in Power sequencing Group D is greater than 10% of its specified minimum operating voltage.

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				FP4 MEMORY INTERFACE	
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DP2 is not support on
FP4 Type 2 processors.

HDMI

eDP

Place resistor(0ohm) for SVT in PWR side

<38> APU_SVT
<38> APU_SVC
<38> APU_SVD

SVCI, SVD1, SVT1
Not support in Type3.

<38> APU_PWRGD
<38> H_PROCHOT#

<38> APU_ALERT#

<38> APU_TDI

<38> APU_TDO

<38> APU_TCK

<38> APU_TMS

<38> APU_TRST#

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<38> APU_TEST53

<38> APU_TEST54

DP_VARY_BL, DP_BLON, DP_DIGON:

Type1&3--> VDD_18

Type2--> VDD_33

UAPU1C

DISPLAY/STAG/TEST

DP_TXP0

DP_TXP1

DP_TXP2

DP_TXP3

DP_TXP4

DP_TXP5

DP_TXP6

DP_TXP7

DP_TXP8

DP_TXP9

DP_TXP10

DP_TXP11

DP_TXP12

DP_TXP13

DP_TXP14

DP_TXP15

DP_TXP16

DP_TXP17

DP_TXP18

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DP_TXP212

DP_TXP213

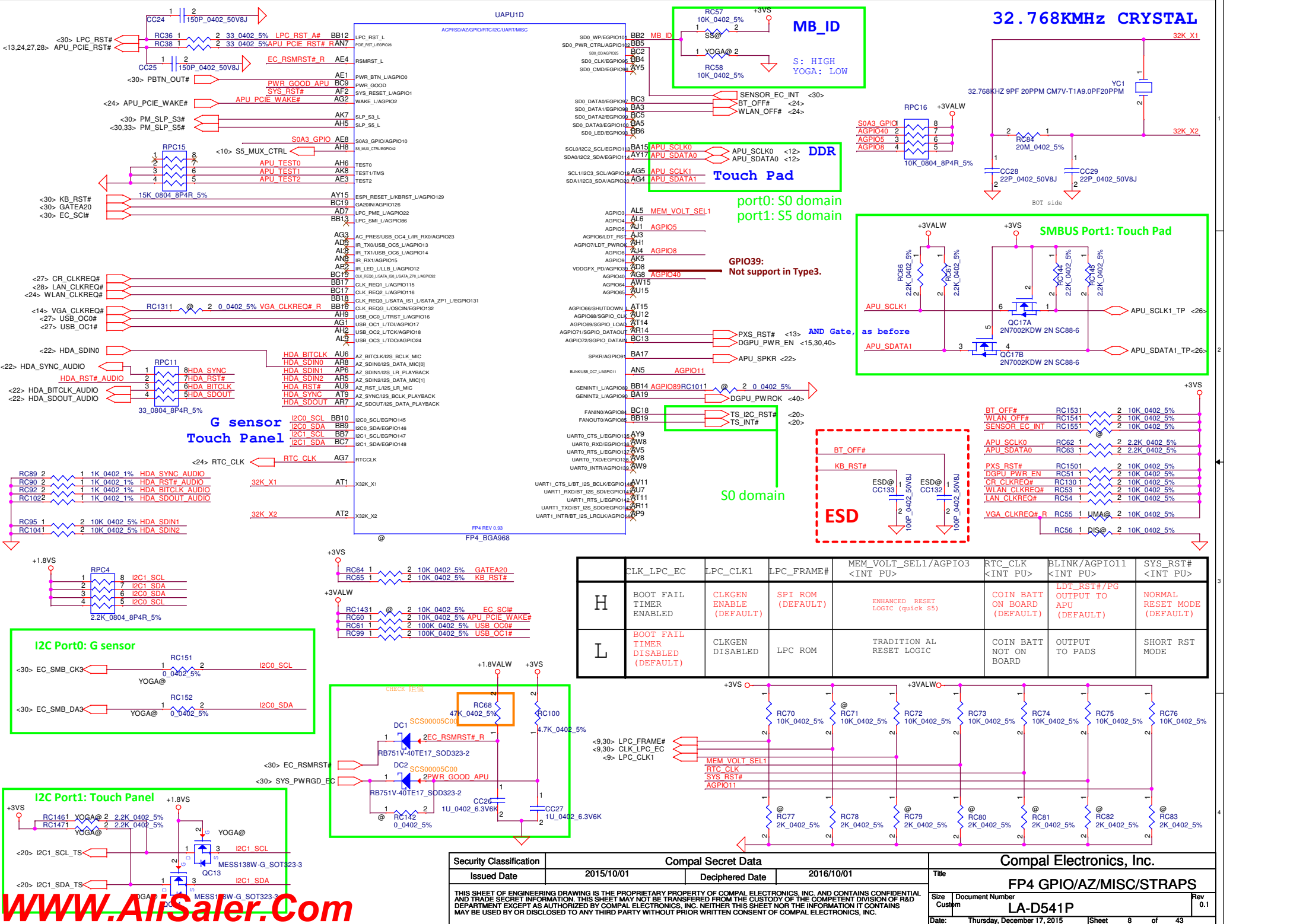
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DP_TXP215

DP_TXP216

DP_TXP217

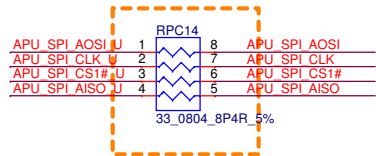
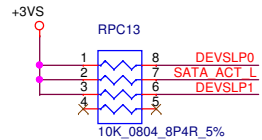
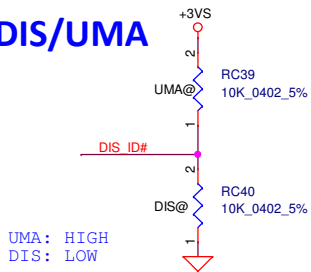
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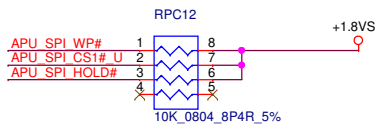
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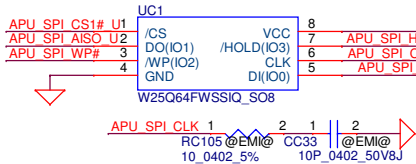
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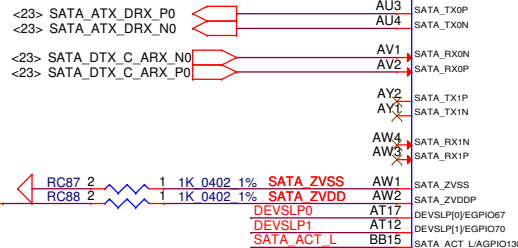
Need check R value



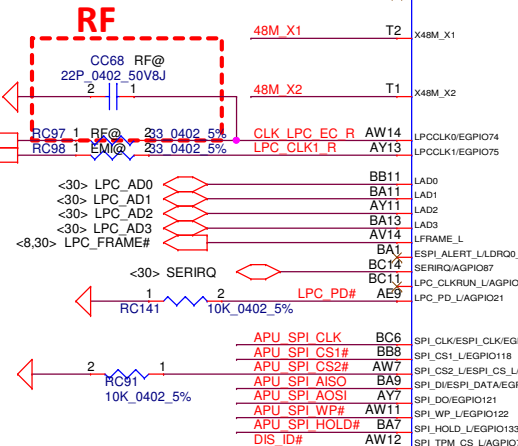
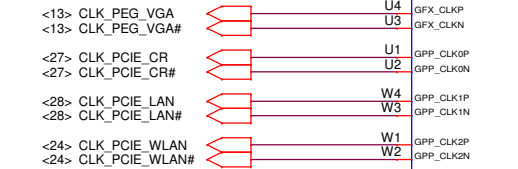
8MB SPI ROM



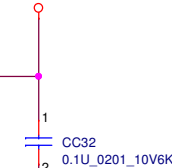
HDD



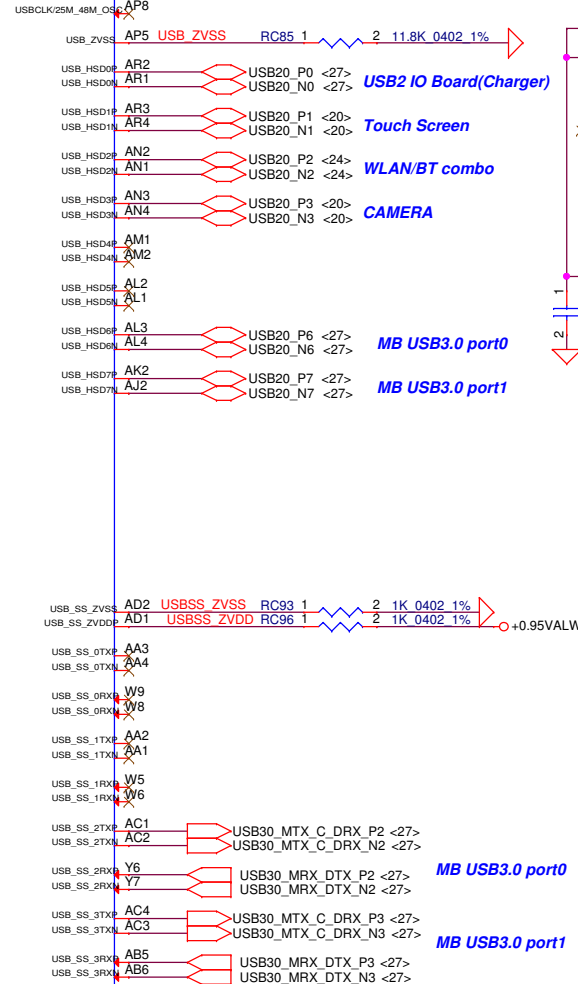
SATA_X1, SATA_X2
Not support in Type3.



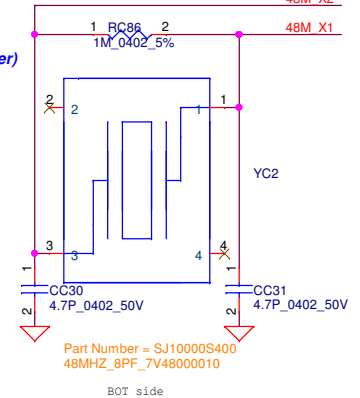
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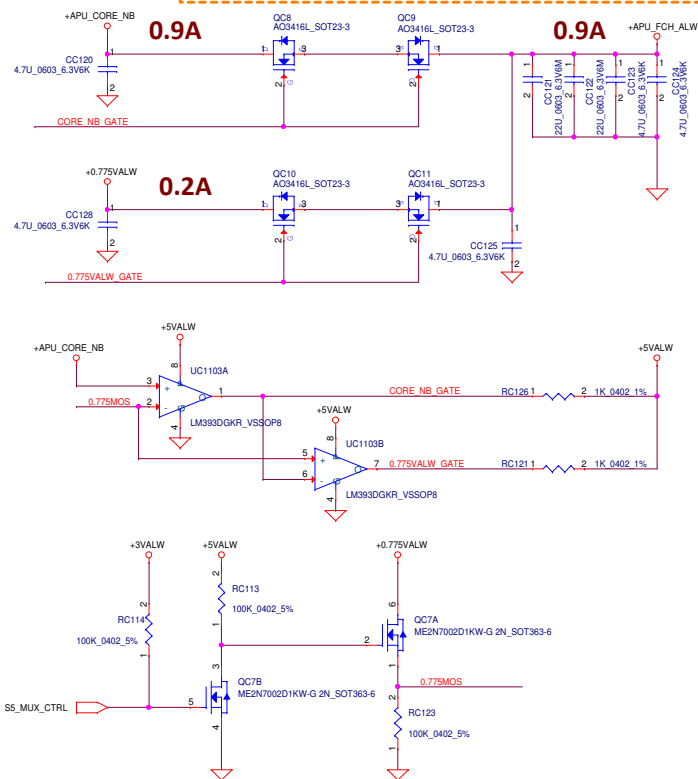
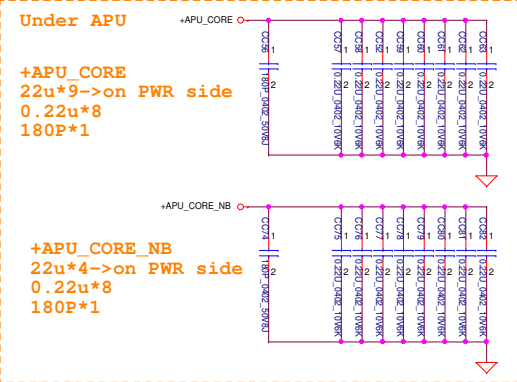
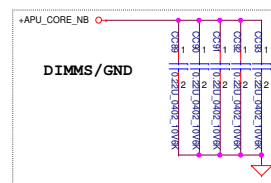
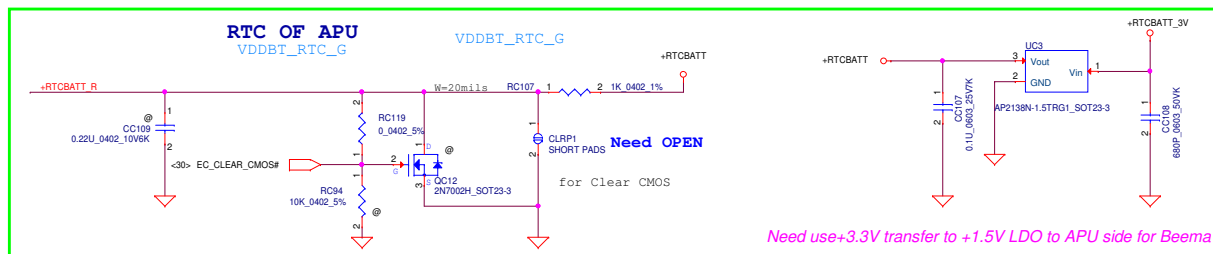
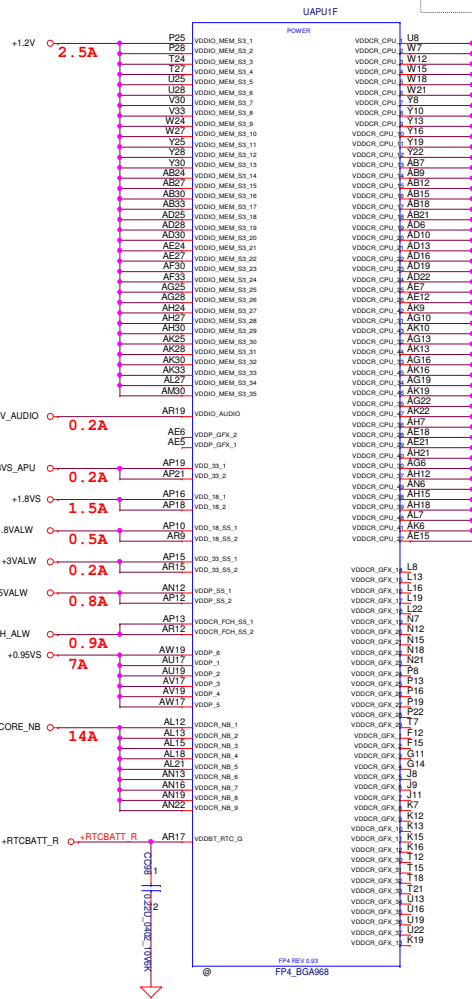
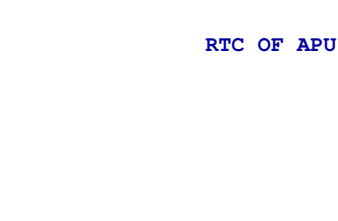
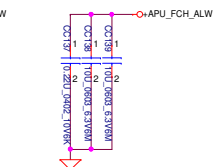
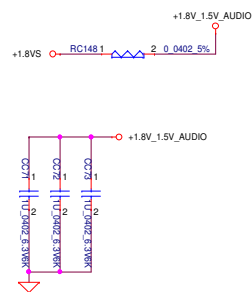
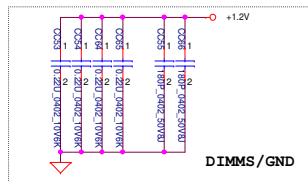
UAPU1E



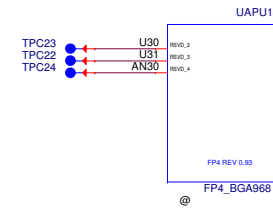
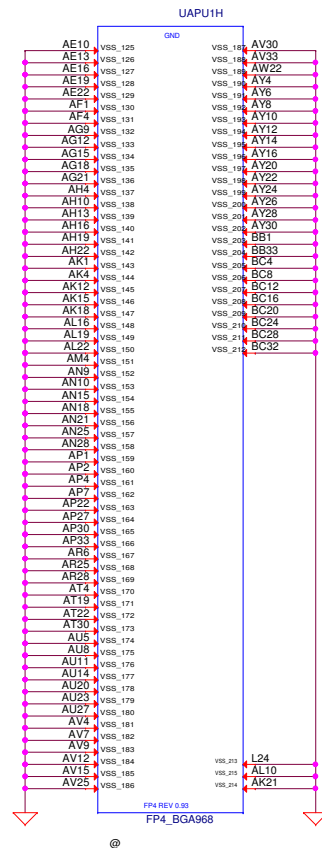
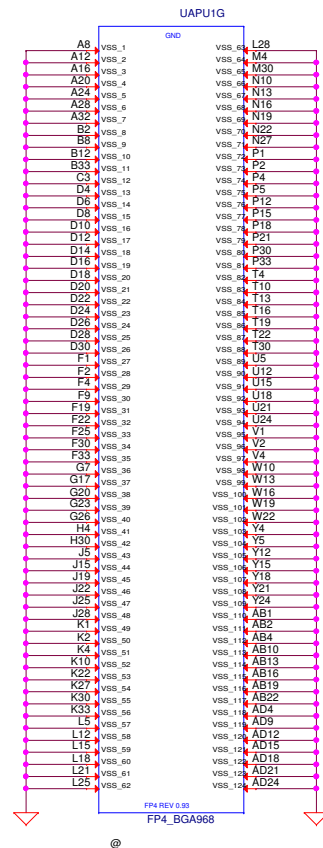
48MHz CRYSTAL



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2016/10/01				2017/10/01				FP4 SATA/CLK/USB/SPI			
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								Document Number		LA-D541P		Rev		0.2	
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								Customer							

Meso/M16M-R16M-M2-50

The following balls cease to work as GPIOs or designated functional pins, and become VDDC:

- GPIO_1
- GPIO_2
- GPIO_14_HPD2
- GPIO_18_HPD3

The following ball ceases to work as a GPIO or designated functional pin, and becomes NC:

- GPIO_7_BLON

The following balls cease to work as GPIOs or designated functional pins, and become NC:

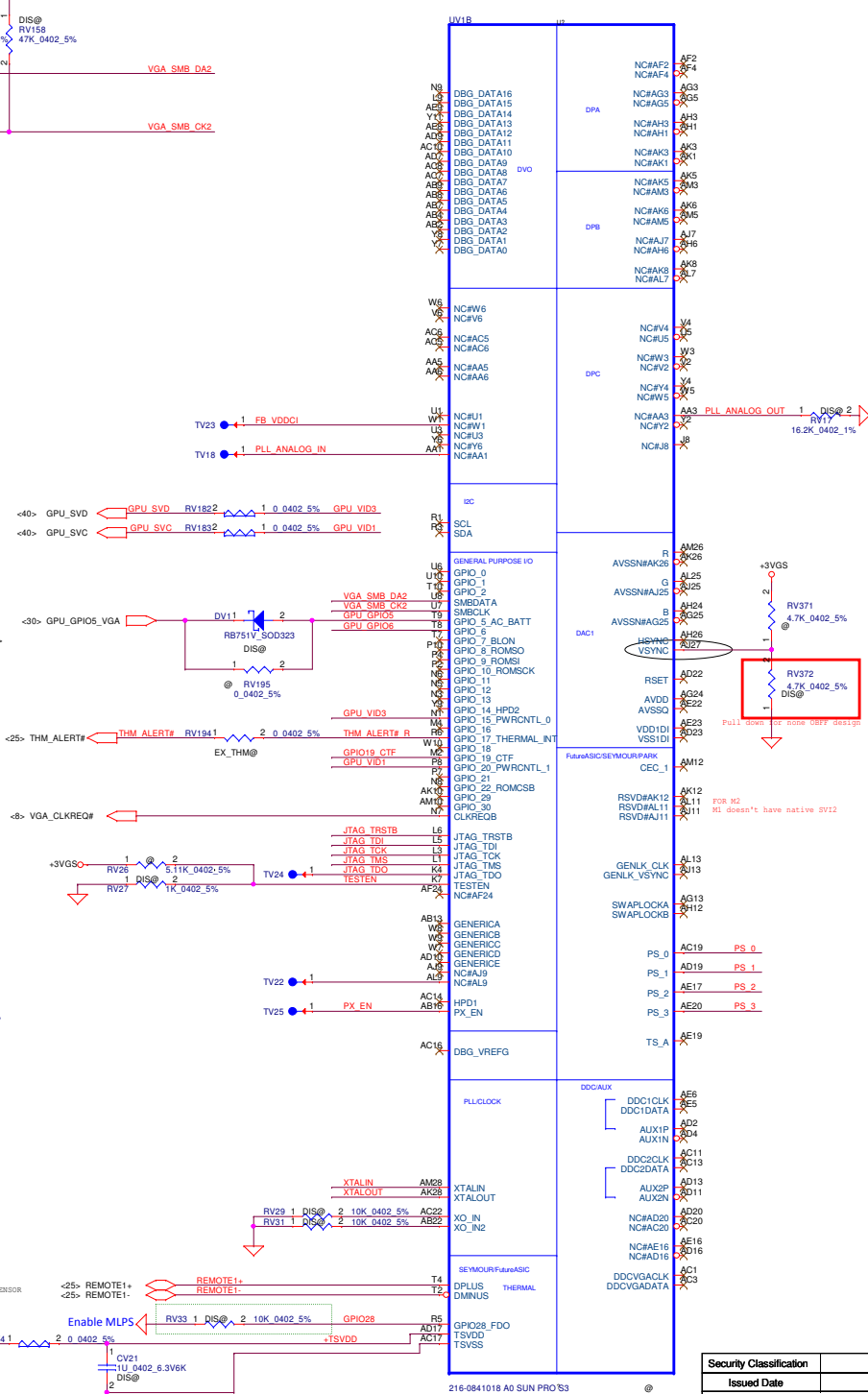
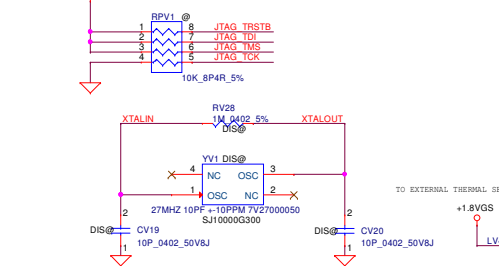
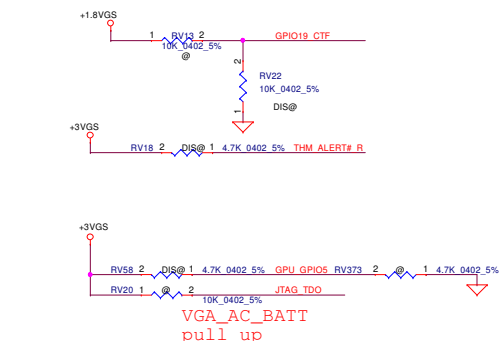
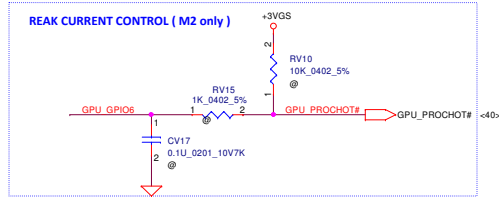
- GPIO_11
- GPIO_12
- GPIO_13
- GPIO_14_HPD2
- GPIO_18_HPD3

"Jet"/"Sun" has a total of 25 VDDC balls. The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun".

"Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36.

The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:

- VARY_BL (AB11)
- DIGON (AB12)
- GENERCA (AB13)
- GENERICC (W9)
- DDC2CLK (AC11)
- DDC2DATA (AC13)
- HPD1 (AC14)
- GPIO_1 (U10)
- GPIO_2 (T10)
- GPIO_18 (W10)
- GPIO_14_HPD2 (Y9)



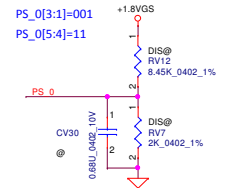
Resistor Divider Lookup Table

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

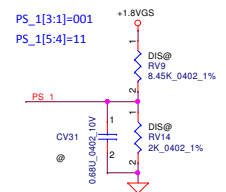
Capacitor Divider Lookup Table

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



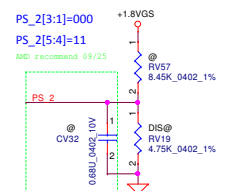
Strap Name:

- PS_0[1] ROM_CONFIG[0]
- PS_0[2] ROM_CONFIG[1]
- PS_0[3] ROM_CONFIG[2]
- PS_0[4] N/A
- PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



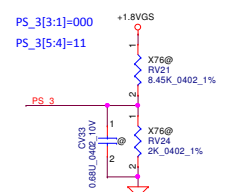
Strap Name:

- PS_1[1] STRAP_BIF_GEN3_EN_A
- PS_1[2] TRAP_BIF_CLK_PM_EN
- PS_1[3] N/A
- PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
- PS_1[5] STRAP_TX_DEEMPH_EN



Strap Name:

- PS_2[1] N/A
- PS_2[2] N/A
- PS_2[3] STRAP_BIOS_ROM_EN
- PS_2[4] STRAP_BIF_VGA_DIS
- PS_2[5] N/A

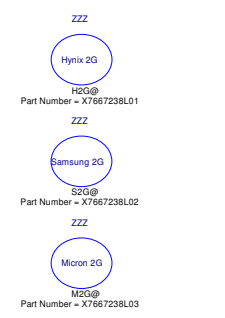
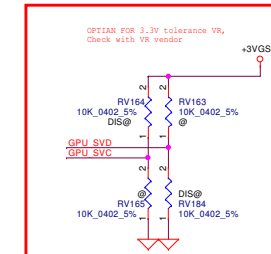


Strap Name:

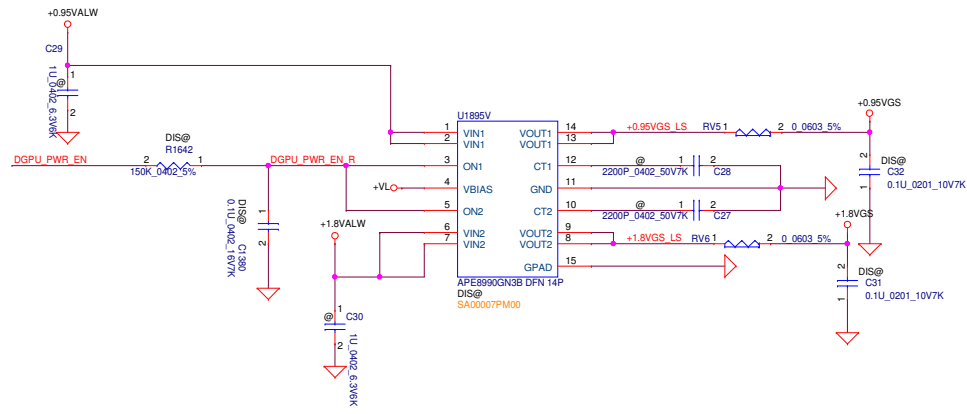
- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

MLPS Memory ID setting:

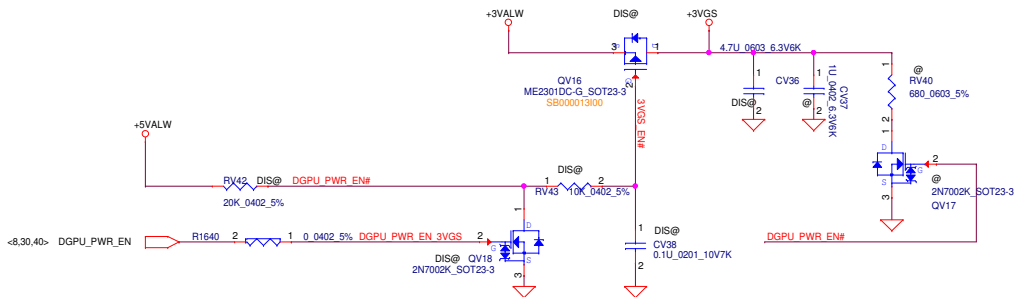
BOARD_CONFIG[2:0]	Memory Type	Configuration	Channel Size	Vendor P/N	SMT quantity	
ID	[2:0]					
0	000	Samsung-DDR3	256M x 16 4PCS, 1 Rank	2GB	K4W4G1646E-BC1A	4pcs
1	001	Hynix-DDR3	256M x 16 4PCS, 1 Rank	2GB	H5TCAG63CFR-N0C	4pcs
2	010	Micron-DDR3	256M x 16 4PCS, 1 Rank	2GB	MT41J256M16LV-091G-N	4pcs



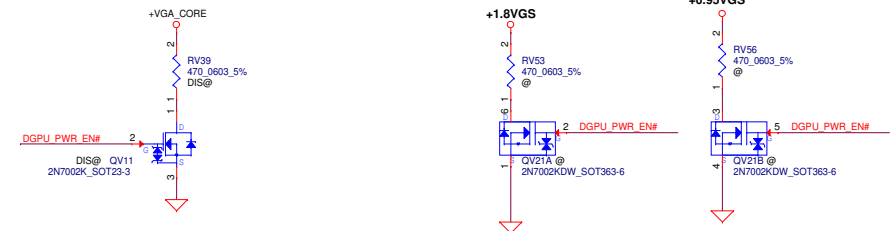
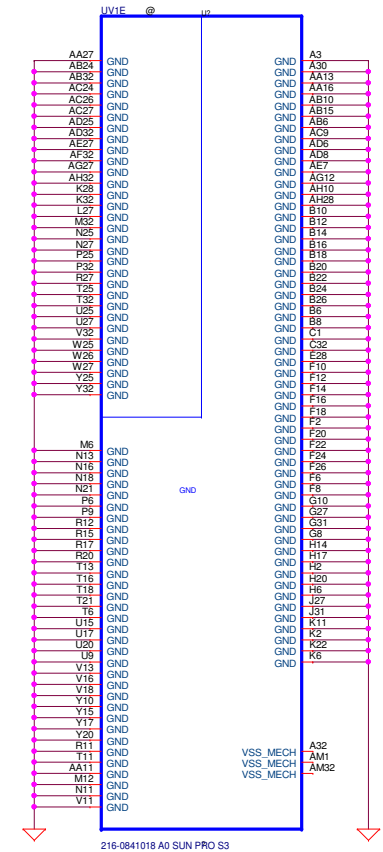
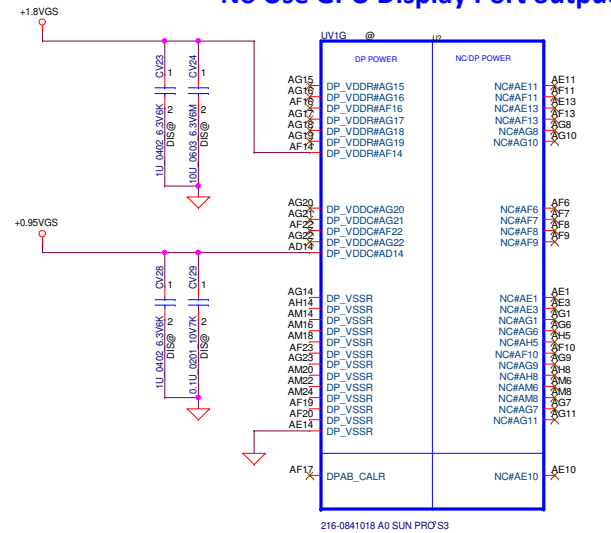
+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch



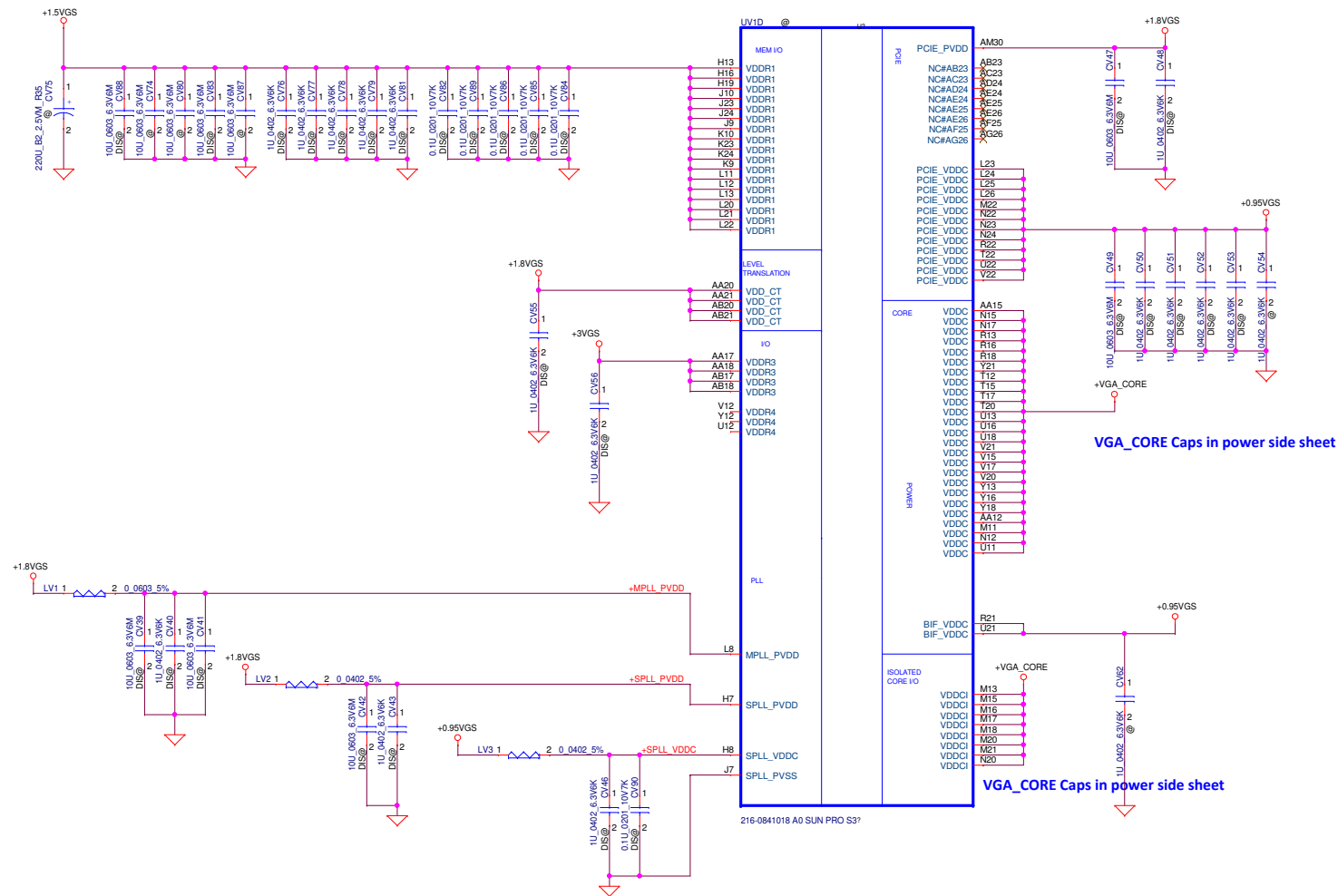
+3VS to +3VGS



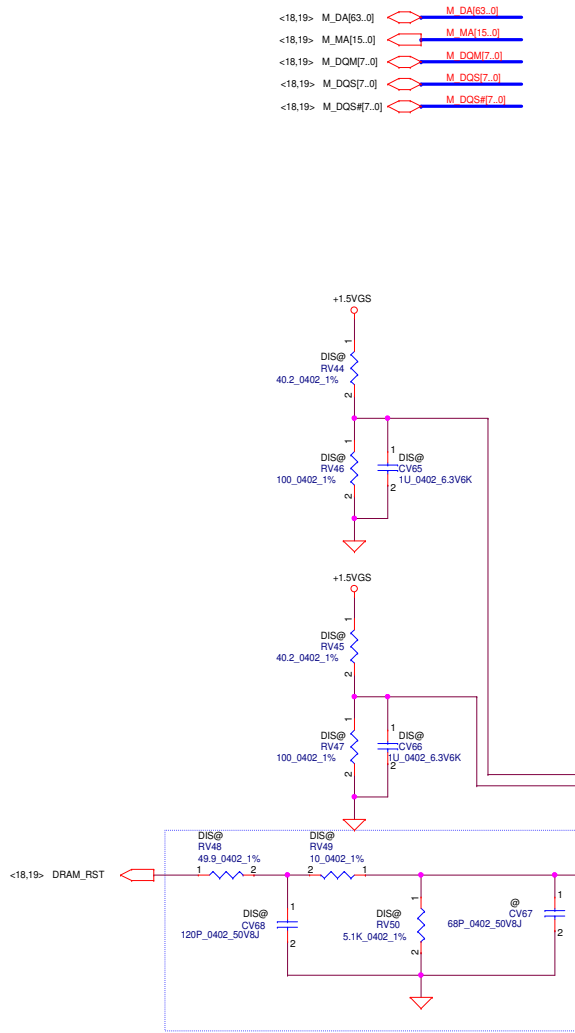
No Use GPU Display Port output



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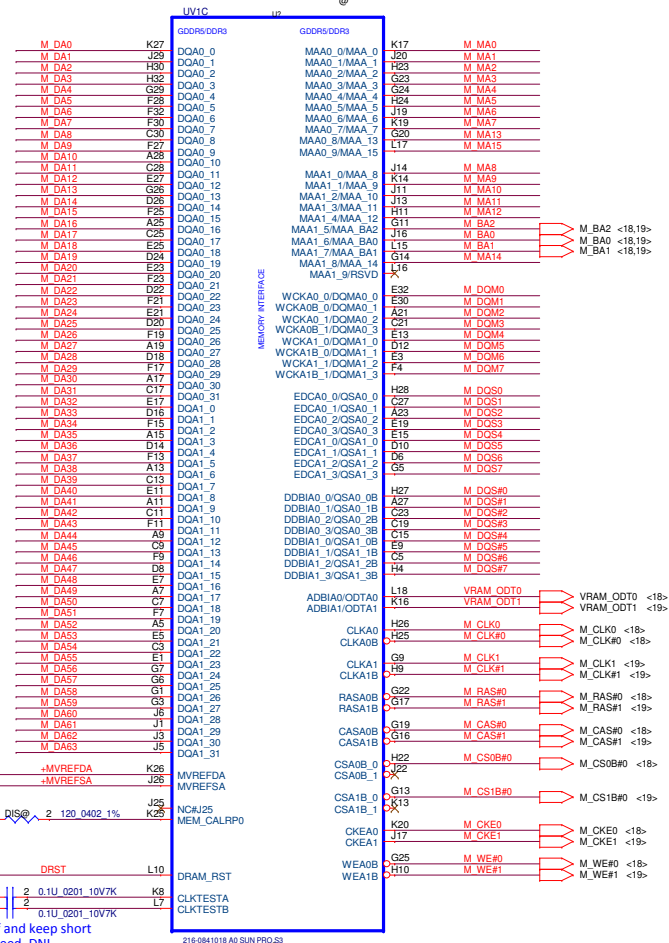


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				Custom	LA-D541P
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				Sheet	16 of 43
				Rev	02



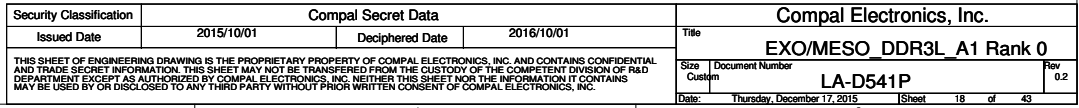
Place close to GPU (within 25mm)
and place component close to each other

Route 50ohms single-ended/100ohm diff and keep short
debug only, for clock observation, if not need, DNI.

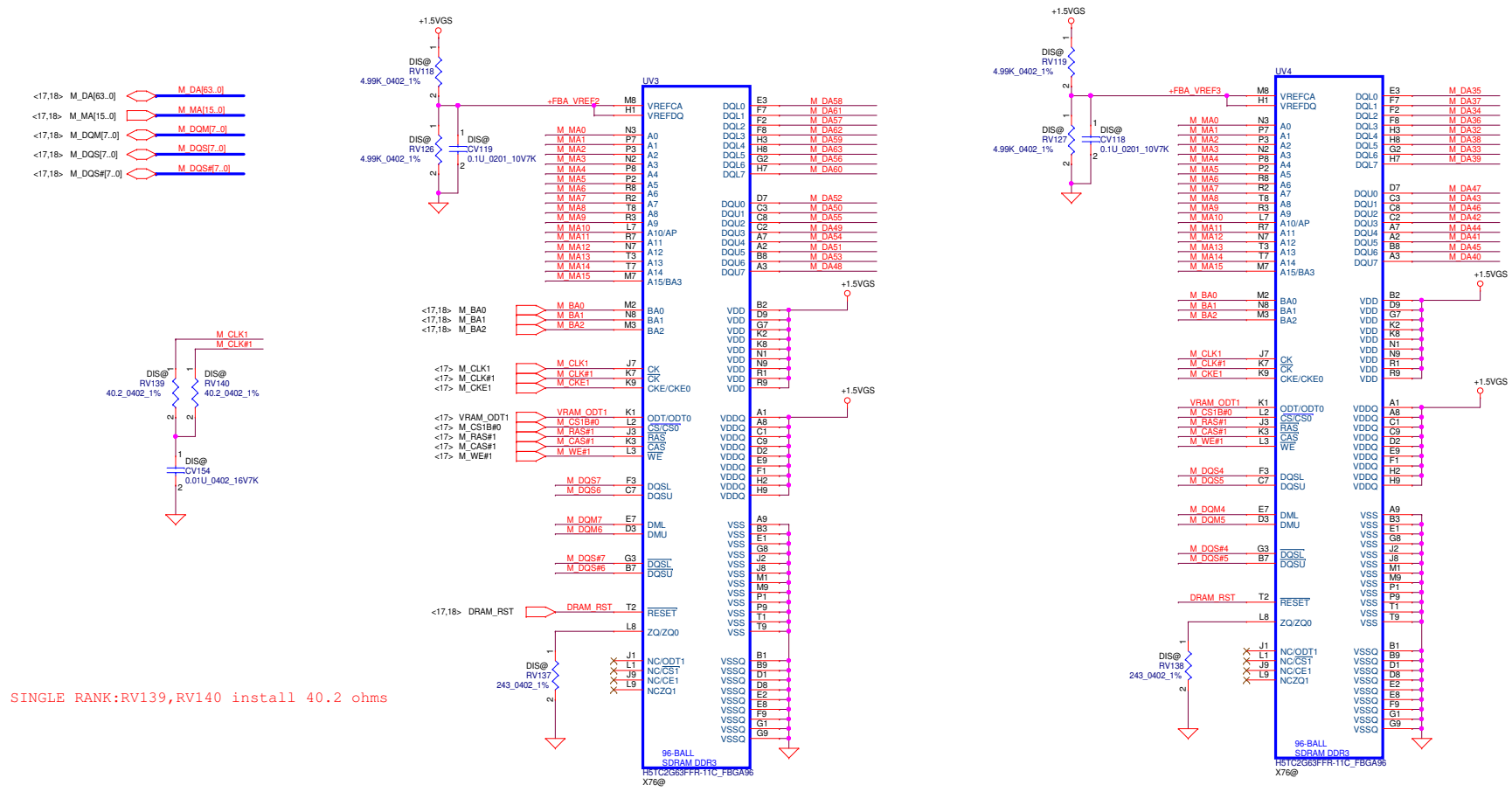


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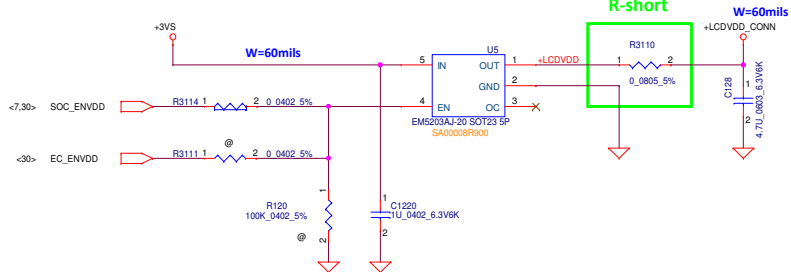
WWW.AliSaler.Com



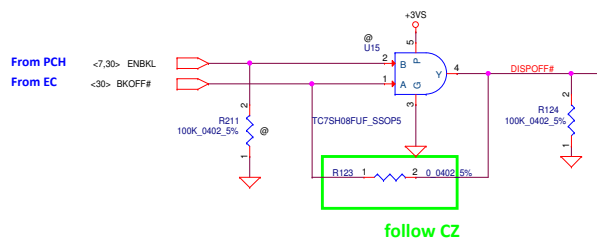
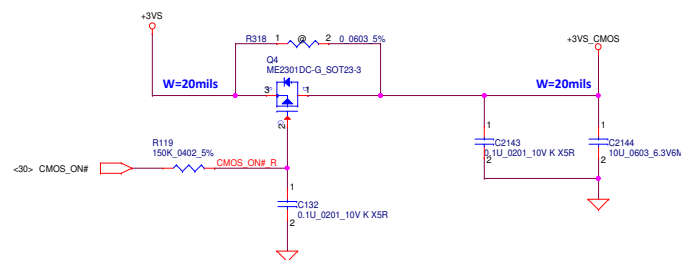
DDR3 Memory Channel Rank 0:A1



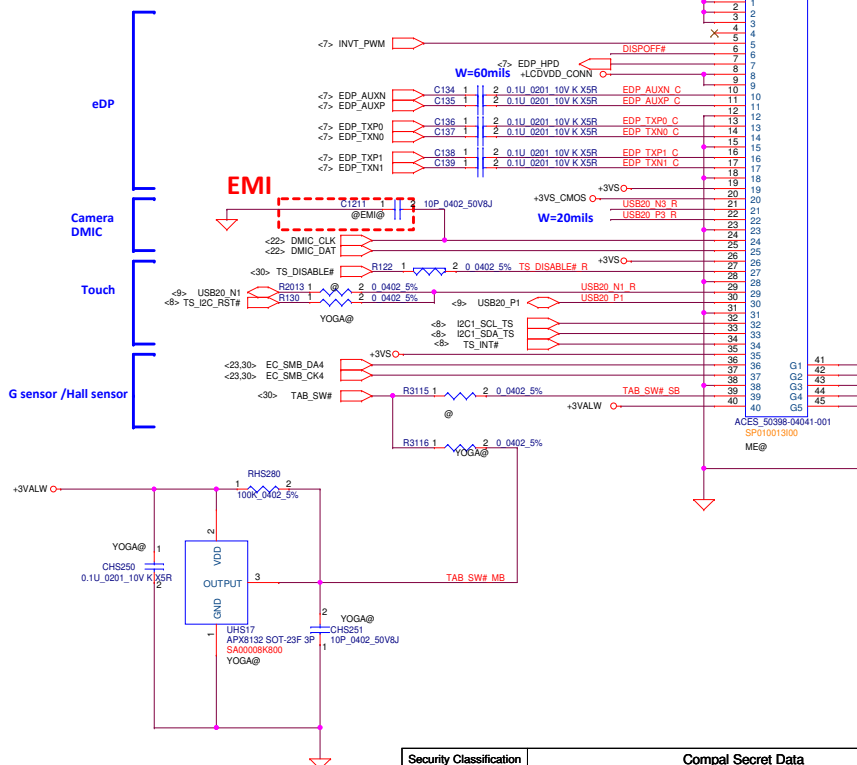
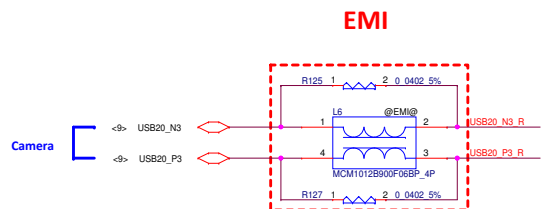
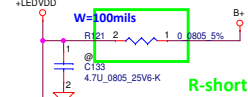
LCD Power Circuit



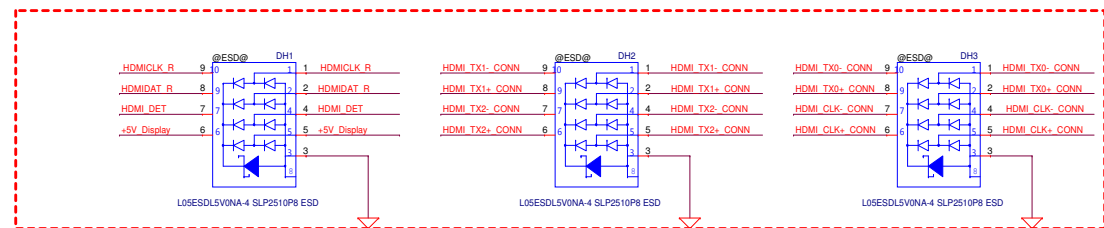
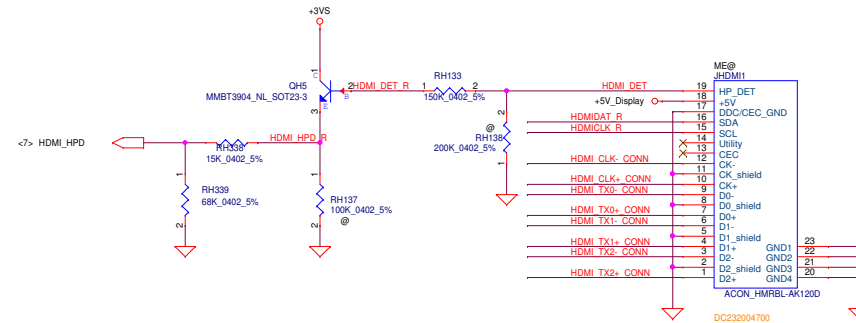
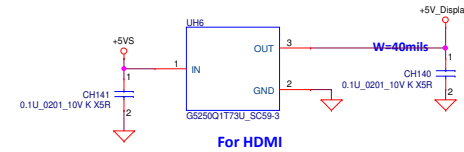
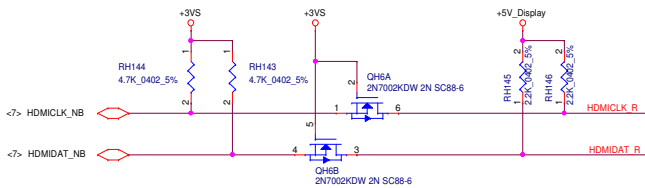
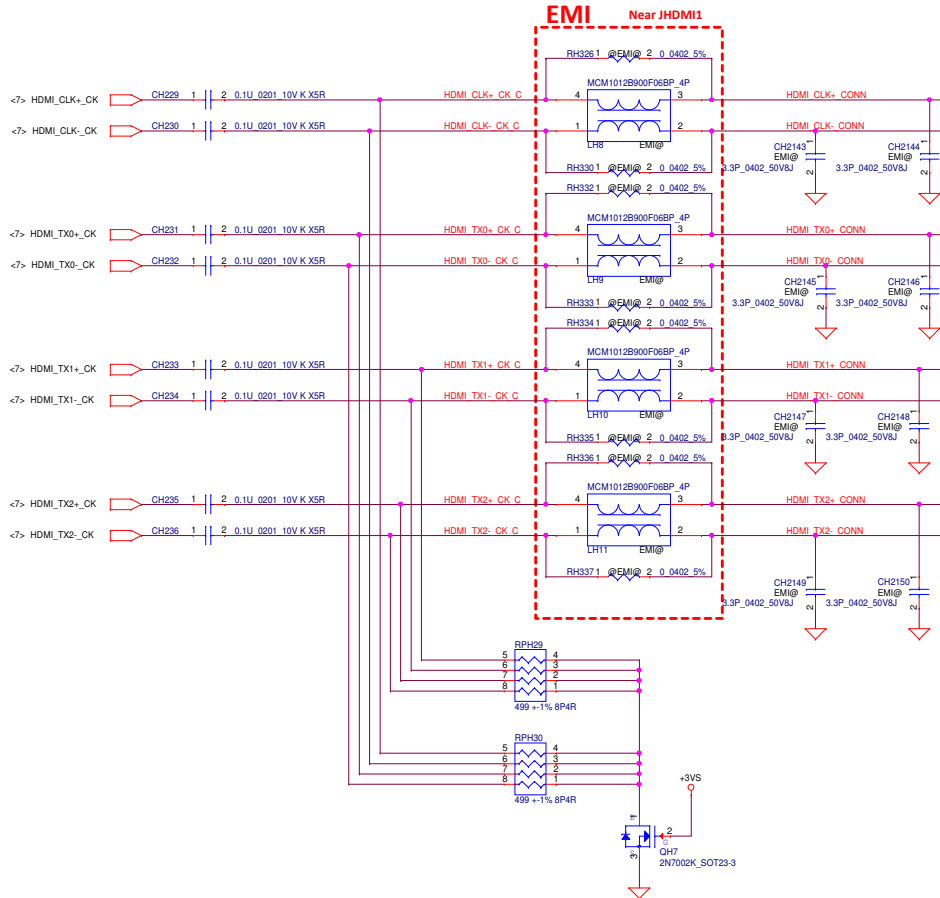
Camera



eDP CONN.

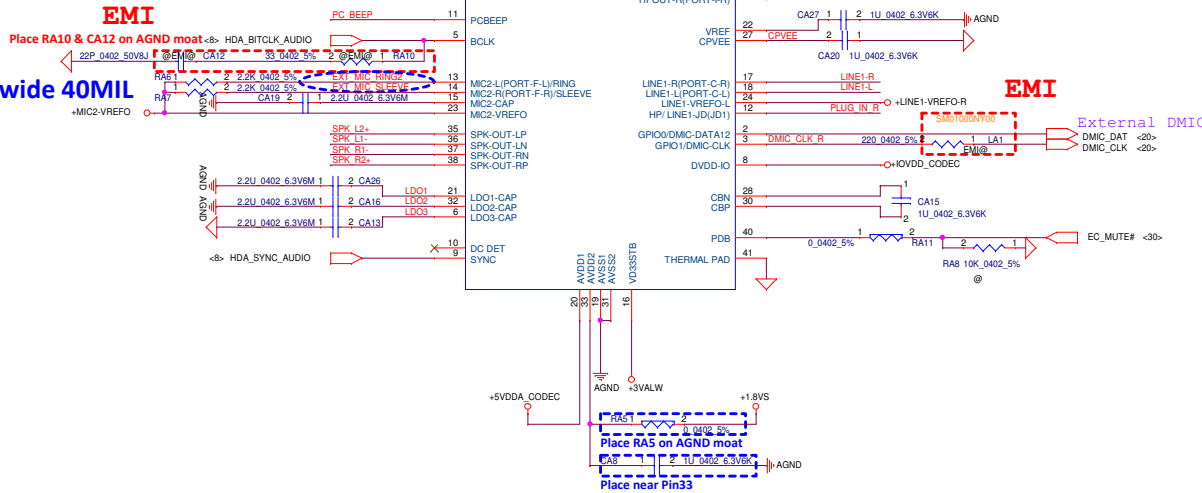


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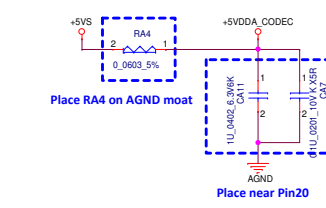


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ALC3240



+5VS → +5VDDA_CODEC



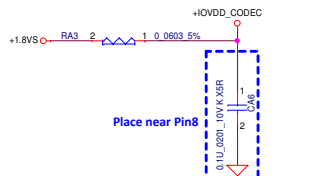
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

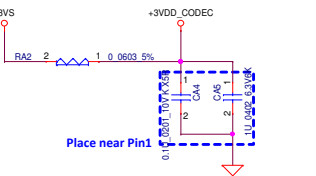
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

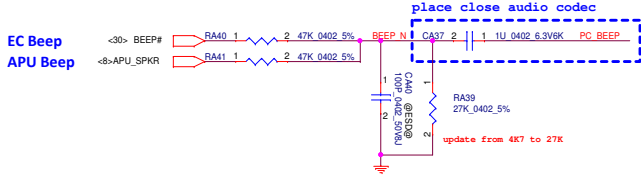
+1.8VS → +IOVDD_CODEC



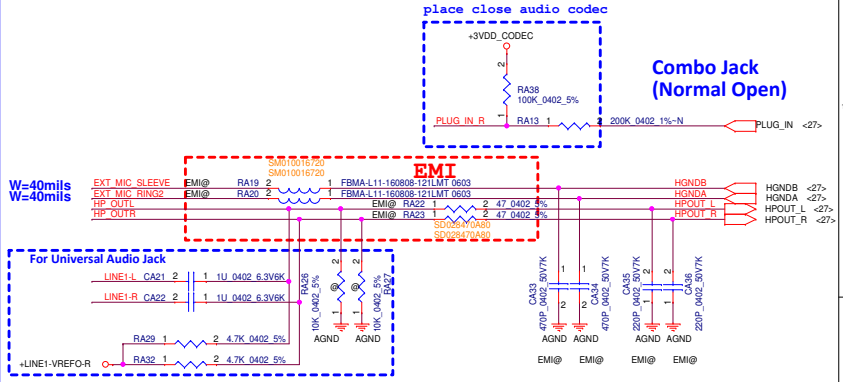
+3VS → +3VDD_CODEC



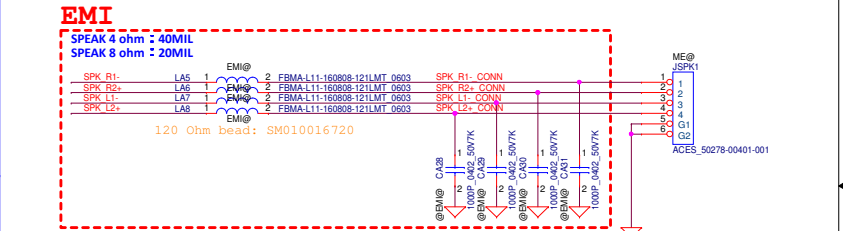
PC BEEP



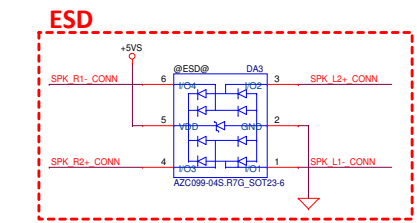
Input



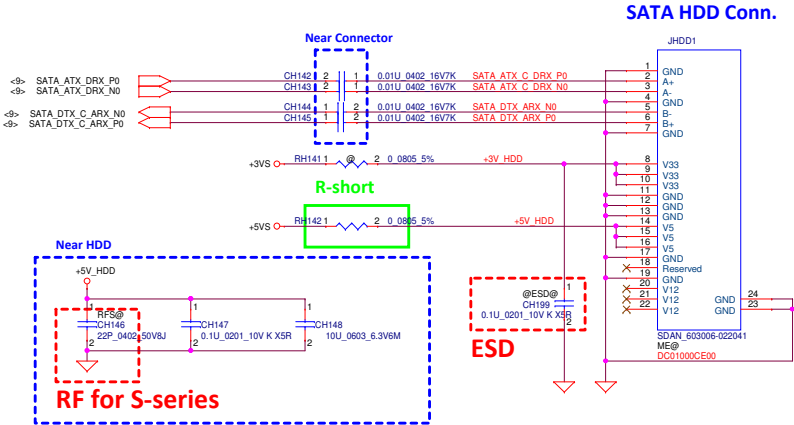
Output



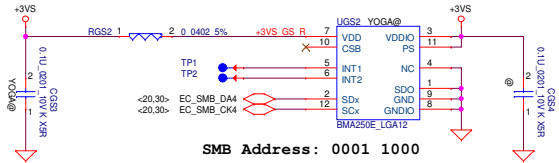
ESD protection needs to be placed near connector side



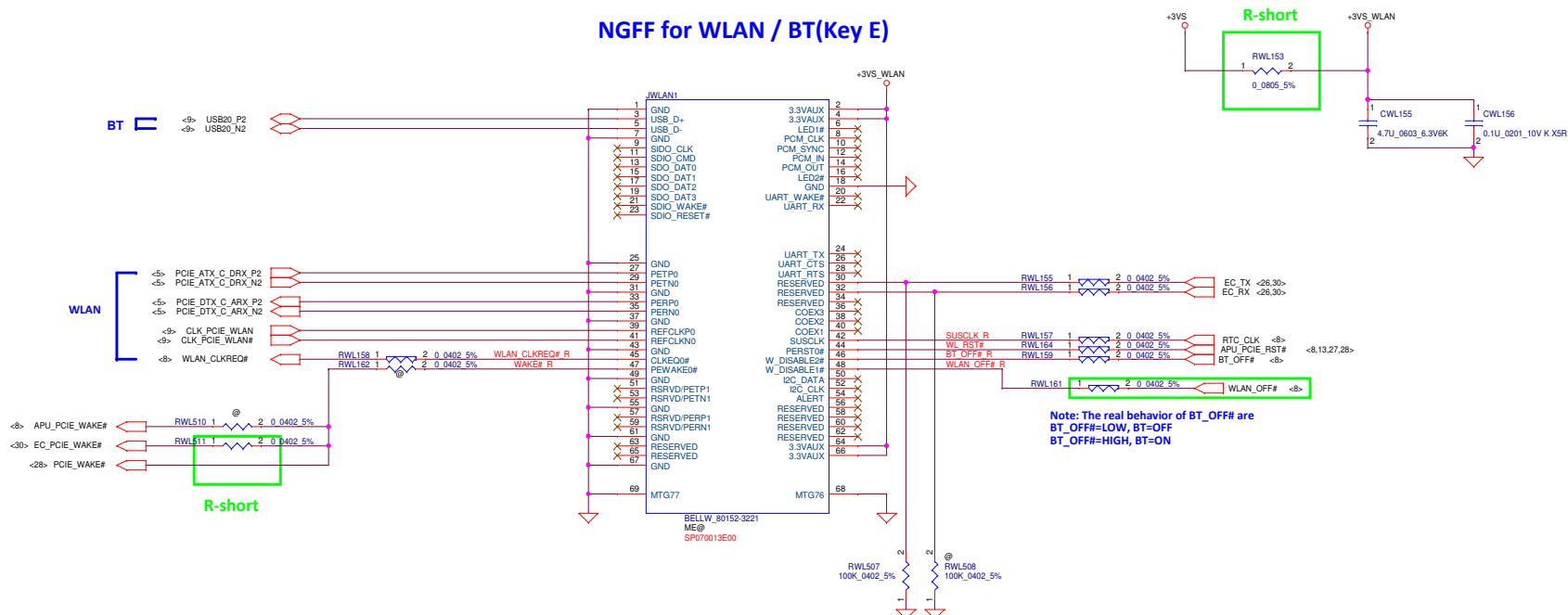
HDD



(G-Sensor for 360-degree reverse)



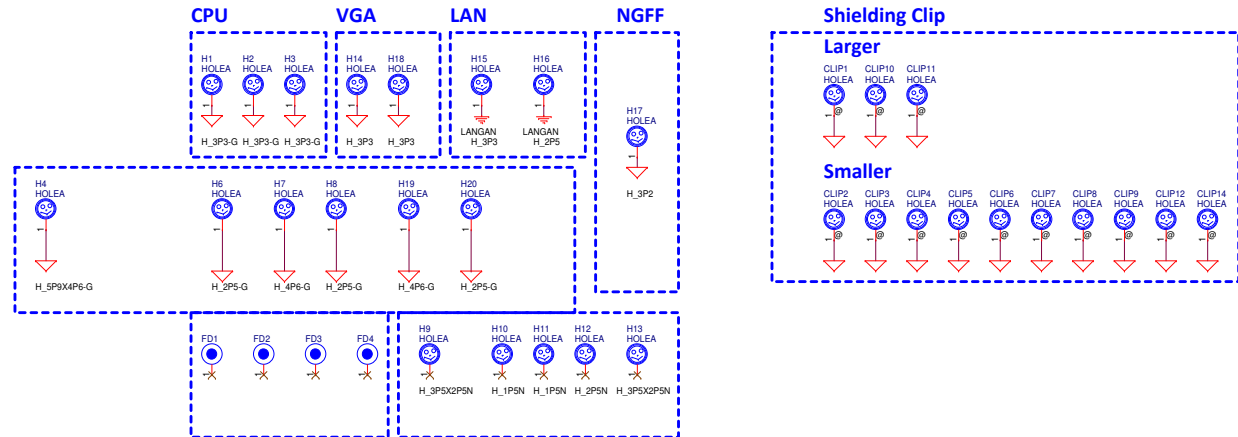
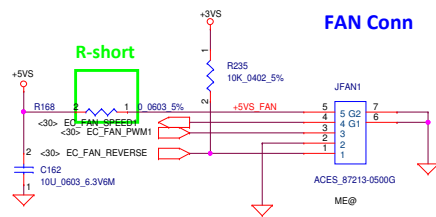
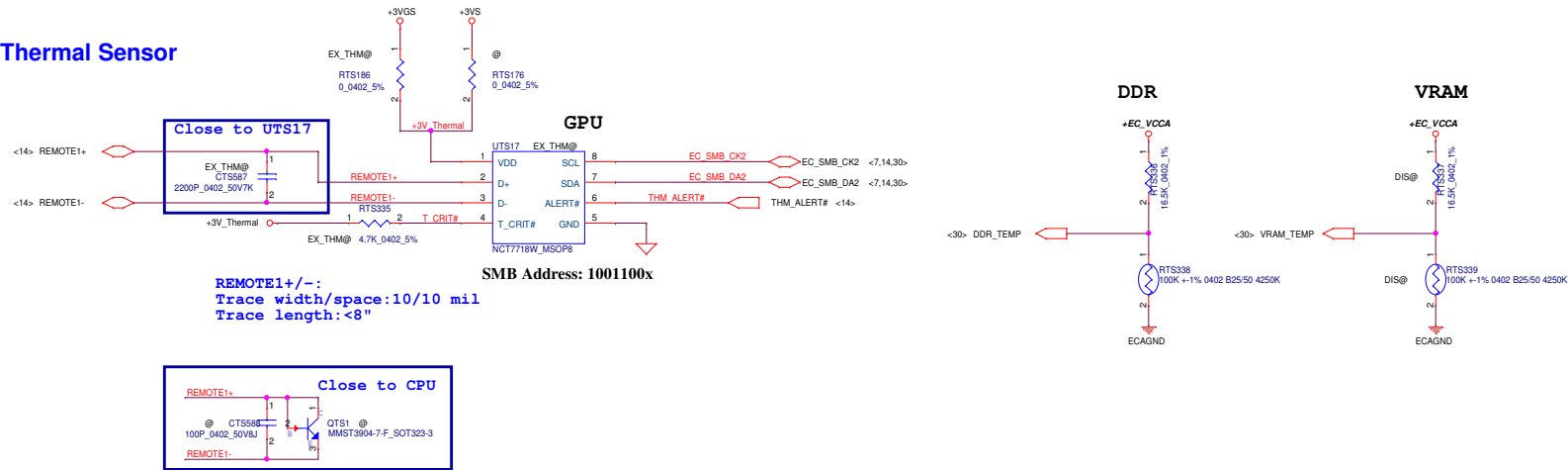
NGFF for WLAN / BT(Key E)



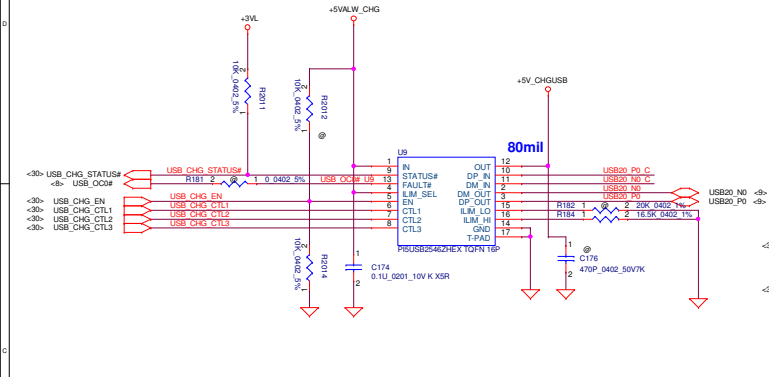
Note: The real behavior of BT_OFF# are
BT_OFF#=LOW, BT=OFF
BT_OFF#=HIGH, BT=ON

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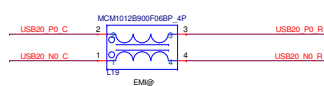
Thermal Sensor



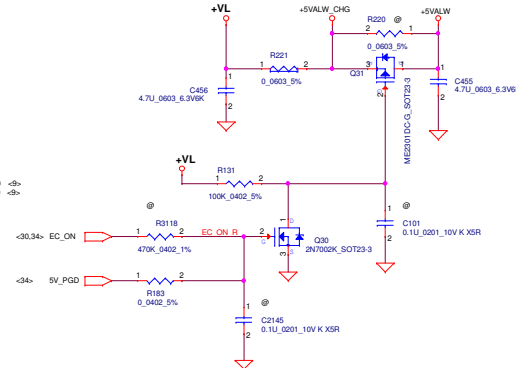
USB Charge



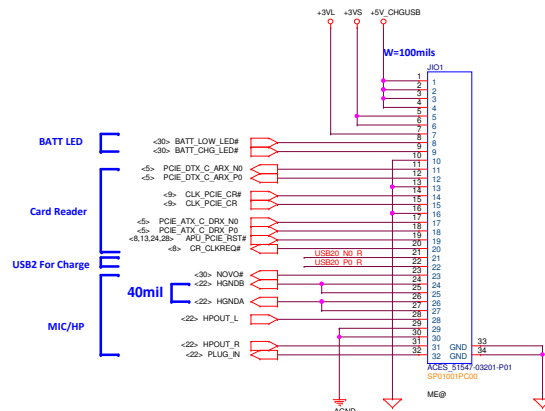
EMI



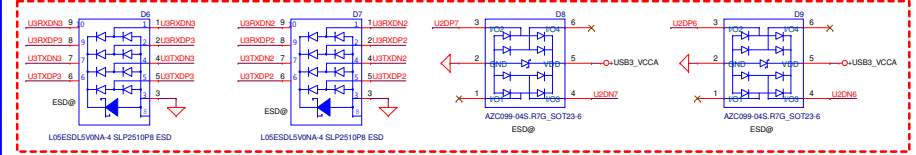
USB Charge switch



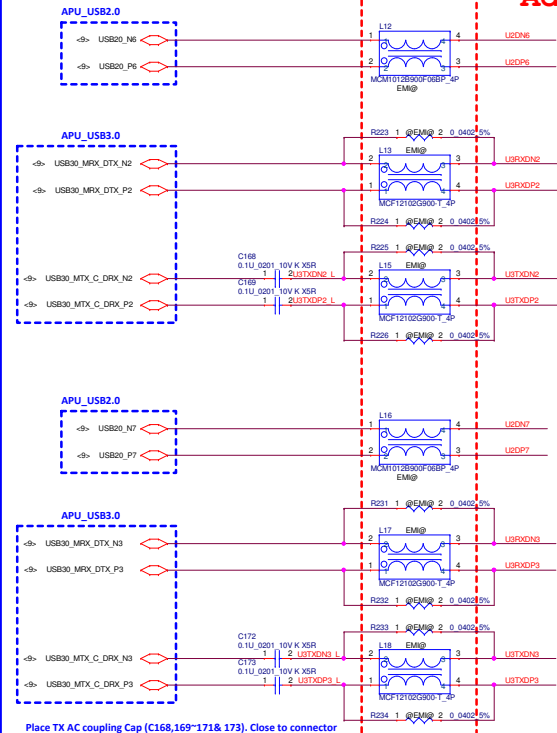
IO CONN



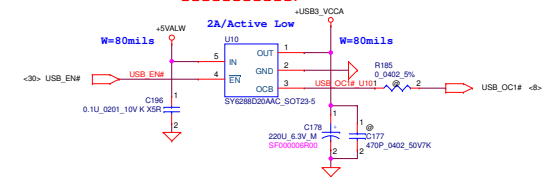
ESD



USB3.0_Port

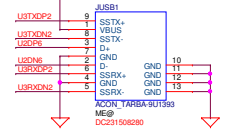


Place TX AC coupling Cap (C168,169~171& 173). Close to connector

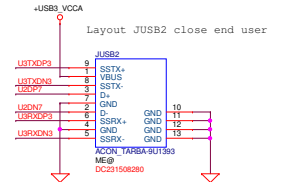


Add resistor

USB3.0 CONN



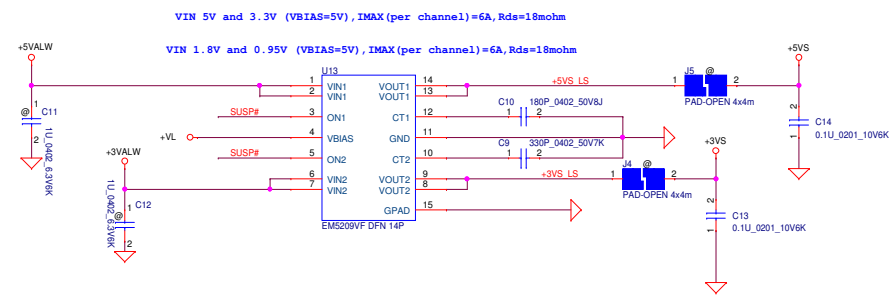
W=80mils



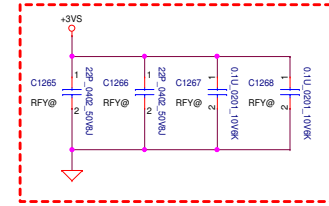
Layout JUSB2 close end user

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Date				Thursday, December 17, 2015				Sheet 27 of 43			

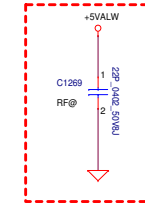
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



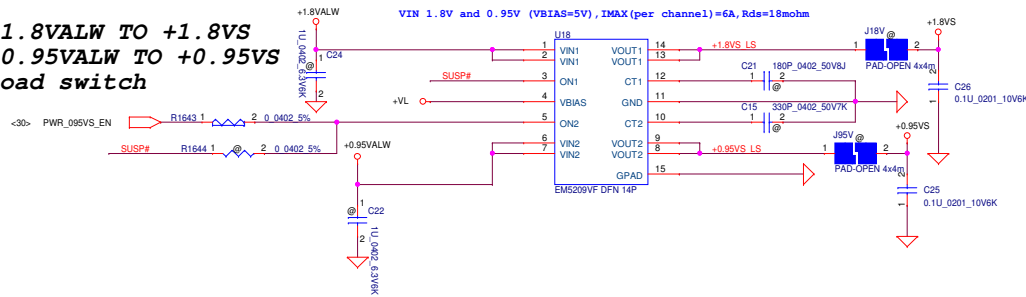
RF for YOGA



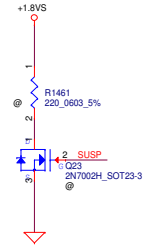
RF



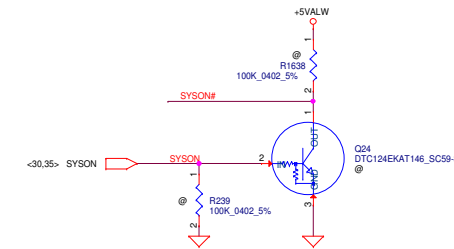
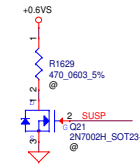
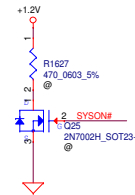
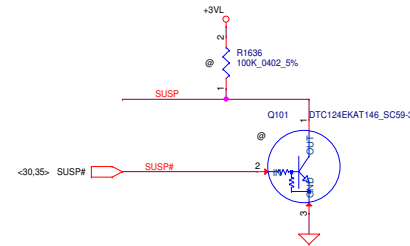
+1.8VALW TO +1.8VS
+0.95VALW TO +0.95VS
Load switch



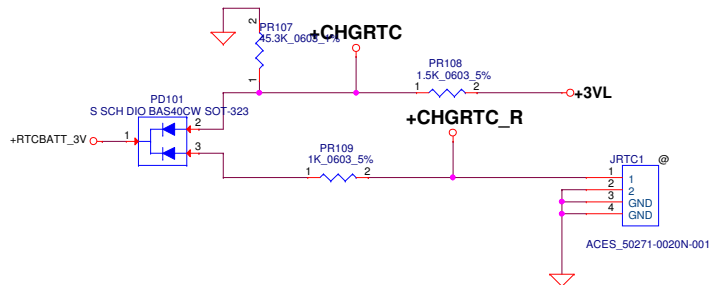
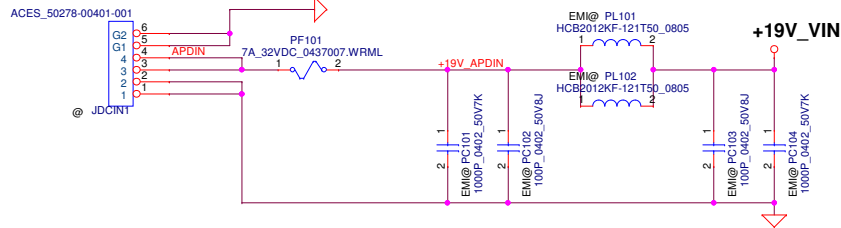
+1.5VS discharge circuit only for Beema
only 1.5VS from PWR



only for Beema



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Size	C	Document Number	LA-D541P		Rev	0.2
Date: Thursday, December 17, 2015				Sheet	29	of 43

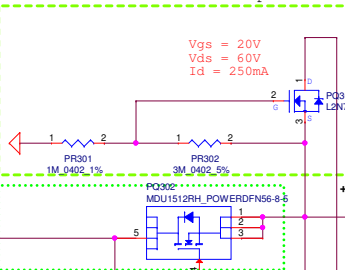


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Issued Date	2015/07/27	Deciphered Date	2016/07/27	PWR- DCIN / Vin Detector	
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33CH <BIT9> PSYS current gain
 R_{s1} = 10mΩ and R_{s2} = 5mΩ or R_{s1} = 10mΩ and R_{s2} = 10mΩ
 BIT0 = 1.14uA/W
 BIT1 = 0.285uA/W
 =====
 R_{s1} = 20mΩ and R_{s2} = 10mΩ or R_{s1} = 20mΩ and R_{s2} = 20mΩ
 BIT0 = 2.28uA/W
 BIT1 = 0.57uA/W

I_{psys} = KPSYS × (VADP × IADP + VBAT × IBAT)
 R_{psys} = 1.2V / I_{psys}
 KPSYS = 1.14uA/W
 adapter wattage = 45W
 Battery wattage = 40Wh
 I_{psys} = 1.14 × (45+40) = 96.9uA
 R_{psys} = 1.2V / 96.9uA = 12.3K-ohm.
 =====
 adapter wattage = 65W
 Battery wattage = 40Wh
 I_{psys} = 1.14 × (65+40) = 119.7uA
 R_{psys} = 1.2V / 96.9uA = 10K-ohm.

Protection for reverse input



V_{gs} = 20V
 V_{ds} = 60V
 I_d = 250mA

R_{ds(on)} = 15.8mohm max
 V_{gs} = 20V
 V_{ds} = 30V
 I_D = 10.5A (Ta=70°C)

max Power loss 0.22W for 90W; 0.12W for 65W system; 0.05W for 45W
 CSR rating: 1W
 VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

PR729 and PR732 are ACDET setting base on your project to set.

support Turbo boost : 2200P
 no support Turbo boost : 0.1u

Follow adapter and battery wattage in V_{sys} current source.
 Base on CPU Core VR design.
 The resistor is pop on CPU VR schematic.

Battery current limited by CCLIM ~ 3.89A.
 Adapter current limited by ACLIM ~ 4.33A.
 (PR719 and PQ741 are for change ACLIM when AC in)

Design Notes
 For 45W/65W /90W system, 2S/3S/4S battery
 Maximum Charging current 3.5A
 Maximum Battery discharge power 55W
 #Register Setting
 1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
 2. Disable turbo when AC only
 #Circuit Design
 1. ACLIM and CCLIM are divider voltage control.
 2. Use 7X7 choke and 3X3 H/L side MOSFET
 Charge current 3A
 Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)
 Power density : 0.61 (23X16)
 #Protect function
 1. ACOPP : VCC voltage > 24V
 2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
 3. ACOC : 0X3CH bit4 set1 release adapter limit function (default:Enable).
 4. CHGOCOP : based on charge current setting
 5. BATOVDP : 4.6V/Cell
 6. BATLOWV : No.
 7. TSHUT : 150C

Module model information
 ISL95520_Hybrid_Boost_V2.mdd

R_{ds(on)} = 32mohm max
 V_{gs} = 20V
 V_{ds} = 30V
 I_D = 8A (Ta=70°C)

R_{ds(on)} = 32mohm max
 V_{gs} = 20V
 V_{ds} = 30V
 I_D = 8A (Ta=70°C)

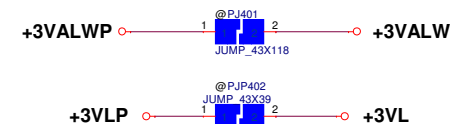
Support max charge 3.5A
 Power loss: 0.245W
 CSR rating: 1W
 VCSPP-VCSIN spec < 81mV

(R_{s1} = 10mΩ and R_{s2} = 5mΩ or R_{s1} = 20mΩ and R_{s2} = 10mΩ).
 CC_LIM = VccLIM / 64 × R_{s2}
 (R_{s1} = 10mΩ and R_{s2} = 10mΩ or R_{s1} = 20mΩ and R_{s2} = 20mΩ).
 CC_LIM = VccLIM / 32 × R_{s2}
 For U22e (65W) and DIS_adp:
 R_{s37}=76.6k
 R_{s37}=76.6k

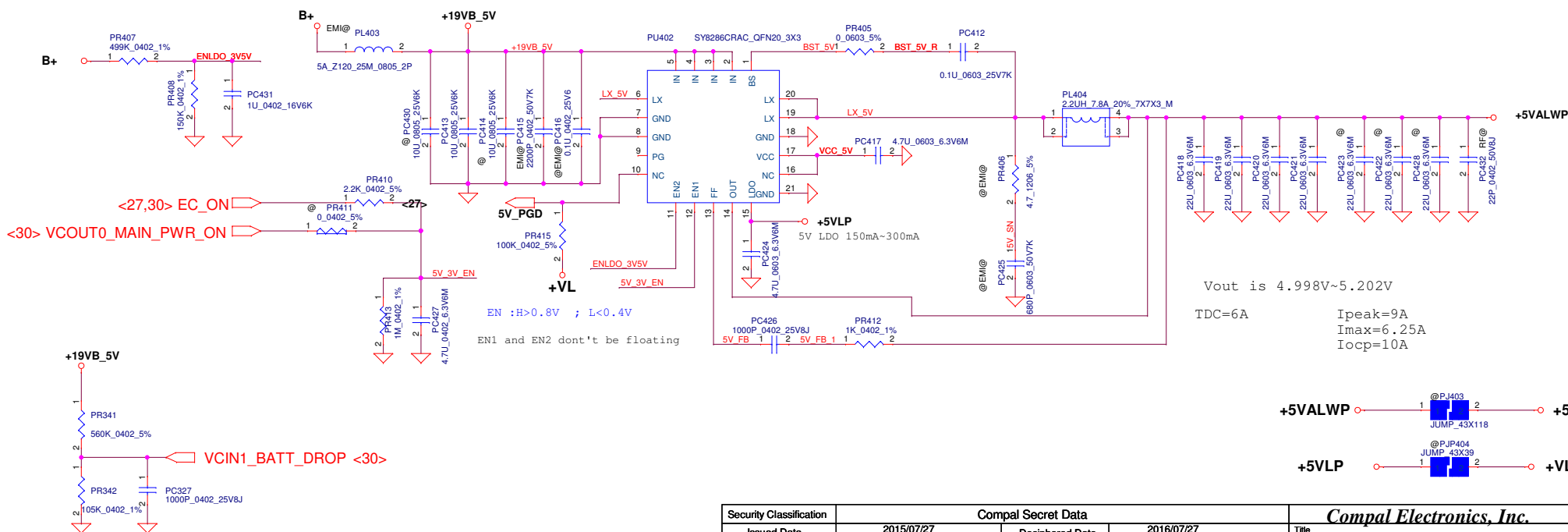
Adapter current limited:
 For U22 (45W)_adp:
 R_{s37}=53.6k
 For U22e (65W) and DIS_adp:
 R_{s37}=76.6k

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Issued Date	2015/07/27	Deciphered Date	2016/07/27	PWR_CHARGER		
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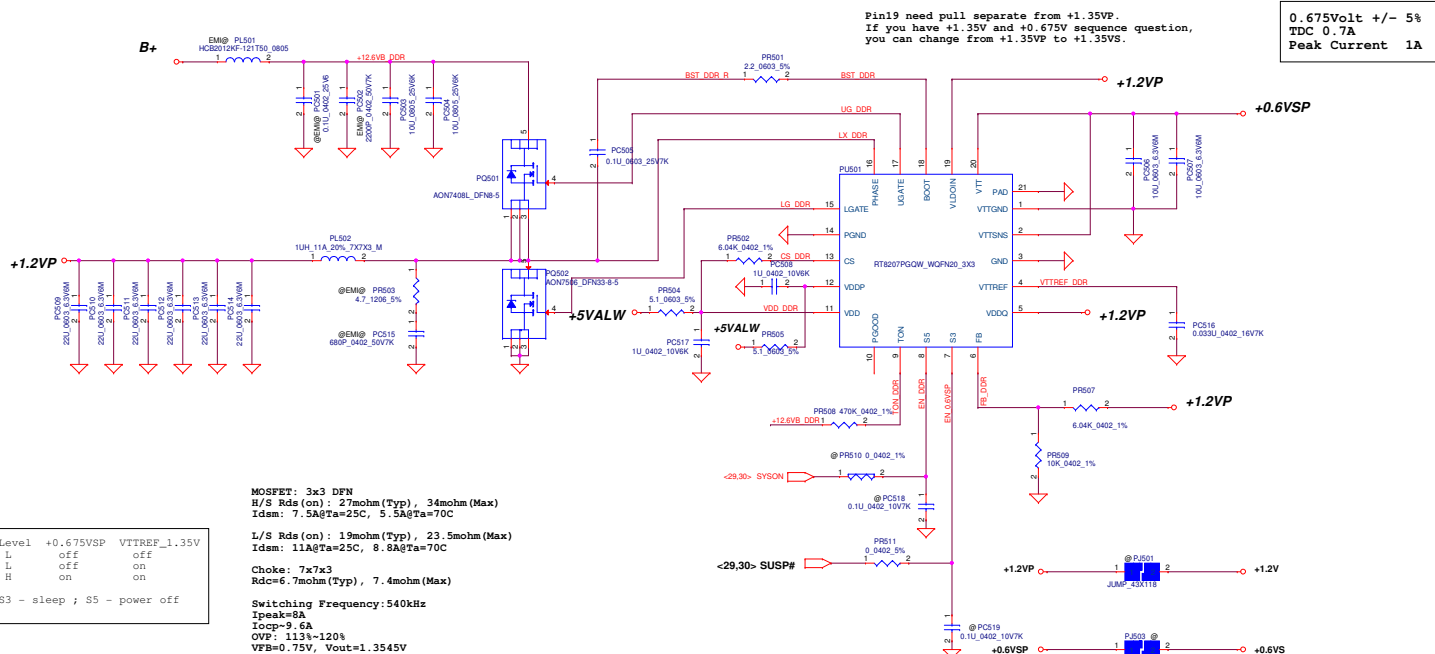
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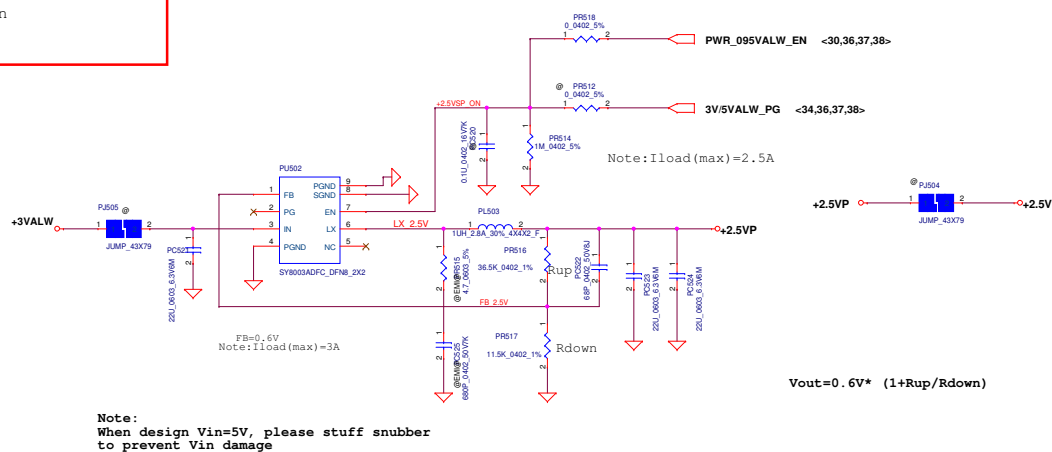
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Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>	
Issued Date	2015/07/27	Deciphered Date	2016/07/27	Title	PWR- 3VALW/5VALW-SY8286B&C
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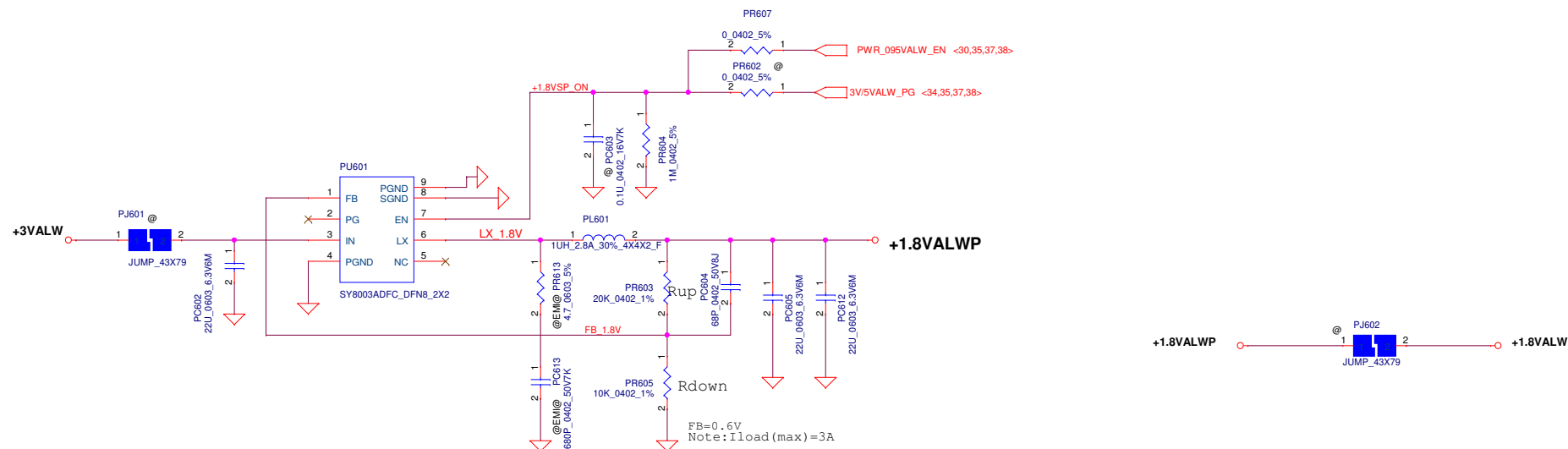
Module model information
SY8003A_V1.mdd



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2015/07/27		2016/07/27		+1.2VP/+0.6VSP/+2.5VP	
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Module model information

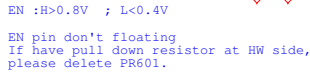
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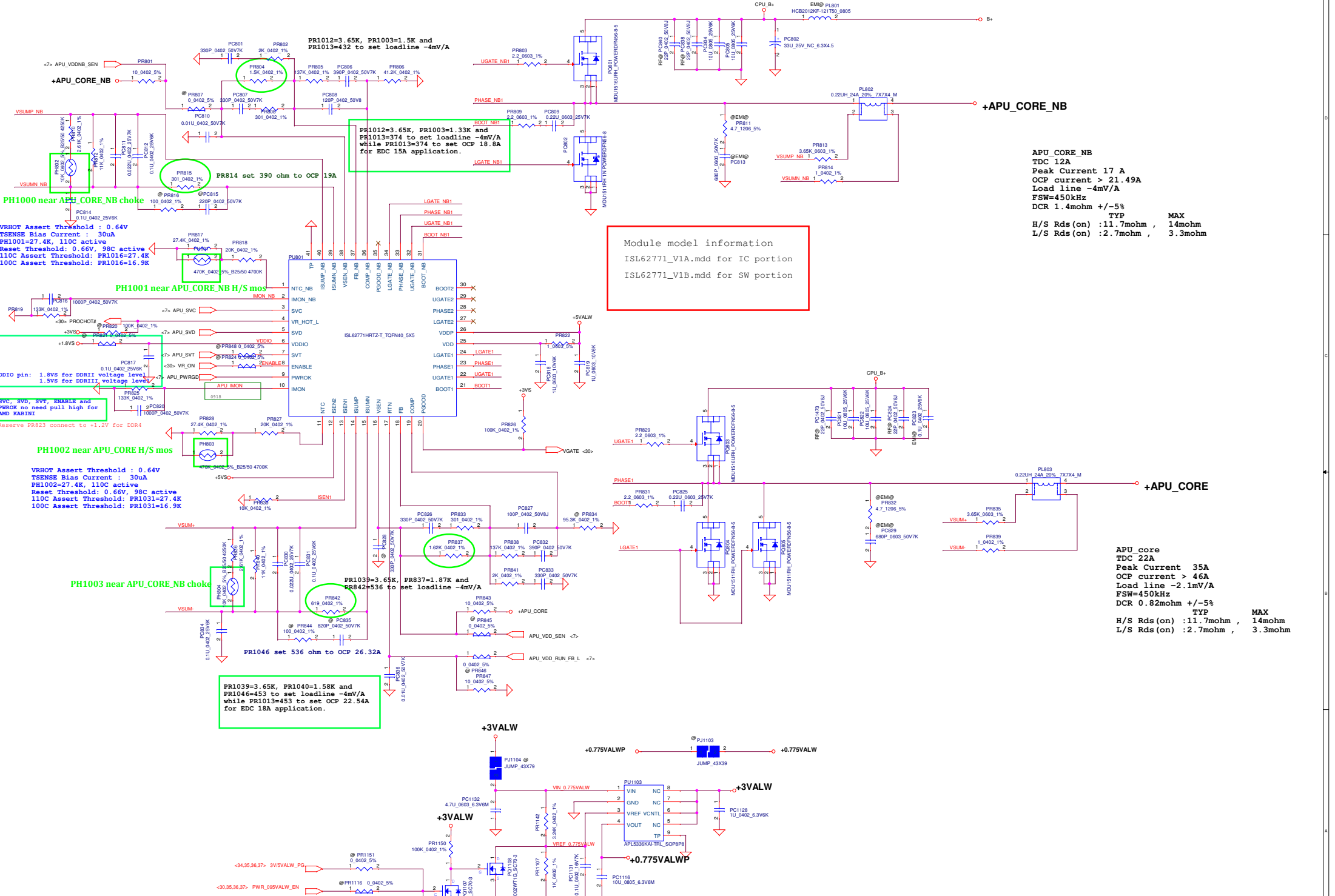
2015/10/28 Delete +1.5VS power rail

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Module model information
SY8288_V1.mdd



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Module model information
ISL62771_V1A.mdd for IC portion
ISL62771_V1B.mdd for SW portion

APU_CORE_NB
TDC 12A
Peak Current 17 A
OCF current > 21.49A
Load line -4mV/A
FSW=450kHz
DCR 1.4mohm +/-5%
TYP
H/S Rds(on) :11.7mohm , MAX 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

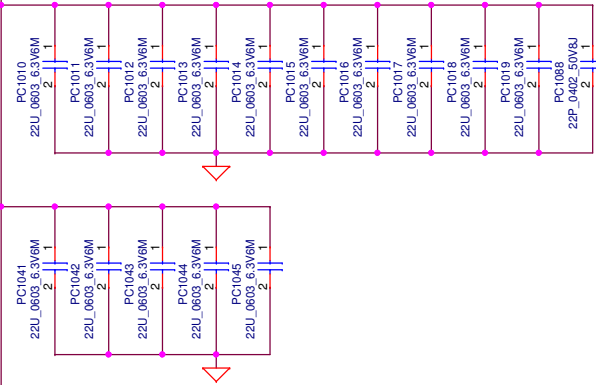
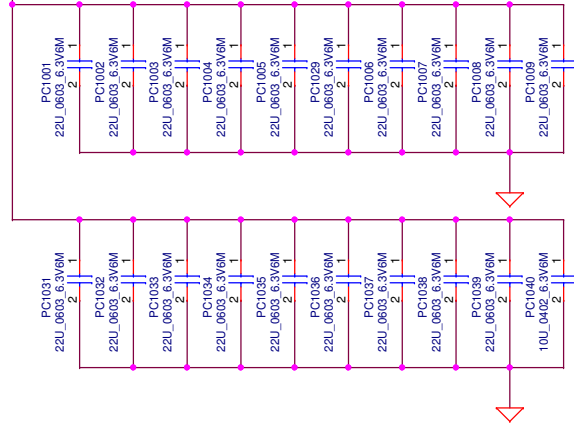
APU_core
TDC 22A
Peak Current 35A
OCF current > 46A
Load line -2.1mV/A
FSW=450kHz
DCR 0.82mohm +/-5%
TYP
H/S Rds(on) :11.7mohm , MAX 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm

+APU_CORE

+APU_CORE_NB

+APU_CORE

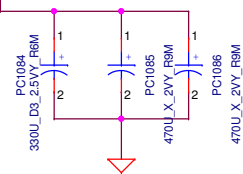
+APU_CORE_NB



APU CORE
470uF*2
330uF*1
22uF*20

APU_CORENB
470uF*1
22uF*15

+APU_CORE



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Size	Document Number	Rev			0.1
Custom					
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Module model information
ISL62771_CZ_GFX35W_V1A.mdd for IC portion
ISL62771_CZ_GFX35W_V1B.mdd for SW portion
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Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modify +1.2V OCP setting	35	Modify PR502 from 13K to 6.04K_0402_1%(SD034604180)	2015/11/03	EVT
2	Modify 0.95V feedback resistor	37	Modify PR705 from 14K to 12K_0402_1%(SD034120280)	2015/11/03	EVT
3	Modify CHARGER COMP	33	Modify PC223 from 0.015U to 0.022U_0402_25V7K(SE075223K80)	2015/11/03	EVT
4	Modify CPU_CORE COMP_NB	38	Modify PR806 from 11.5K to 41.2K_0402_1%(SD000009K00)	2015/11/03	EVT
5	Modify CPU_CORE COMP	38	Modify PC827 from 68P to 100P_0402_50V8J(SE071101J80) Modify PR834 to un-mount	2015/11/03	EVT
6	Modify VGA_CORE ISUMN	40	Modify PR1427 from 604 to 549_0402_1%(SD034549080)	2015/11/03	EVT
7	Modify VGA_CORE Rdroop	40	Modify PR1424 from 2.1K to 1.37K_0402_1%(SD034137180)	2015/11/04	EVT
8	Modify +0.95VALW output capacitor	37	Add PC714 & PC715(22U_0603_6.3V6M)	2015/11/04	EVT
9	Modify capacitor size	38	PC812 & PC814 & PC831 & PC834 change from 0603 to 0.1U_0402_25V6K (SE00000G880)	2015/11/06	EVT
10	Modify 0 ohm P/N	35	PR511 change from to 0_0402_1% to 0_0402_5%(SD028000080)	2015/11/09	EVT
11	Modify APU CORE IC VDDIO for DDR4 design	38	Change PR821 to 0_0402_5%(SD028000080) Reserve PR823 connect to +1.2V for DDR4	2015/11/10	EVT
12	PSYS add 0ohm connect to GND for AMD platform	33	PR322 change to 0_0402_5%((SD028000080))	2015/11/12	EVT
13	Change VGA CHOKE for thermal team request	40	Change PL1402 & PL1403 from 0.24UH_22A_+-20%_7X7X3_M(SH000010N00) to 0.22UH_24A_20%_ 7X7X4_M(SH000011H00)	2015/11/12	EVT
14	Modify DGPU_PWR_EN sequence for GPU CORE IC	40	Add PC1472 (0.22U_0402_10V6K, SE095224K00) Change PR1444 from 0_0402_5%(SD028000080) to 100K_0402_5%(SD028100380)	2015/11/12	EVT
15	Modify VGA CHOKE location	40	Change location from PL1406 to PL1403	2015/11/18	EVT
16	Add EMI solution		1.PJ301 change to PL301 ISN CHOKE(SH00000YG00) 2.PJ701 change to PL701 EMI bead(SM01000P200) 3.PR312 change from 0_0603_5% to 2.2_0603_5% 4.Add PR317 , PC217 , PC205	2015/12/03	DVT
17	To avoid VL protection for HW USB CHG	34	1.Add PC431(1U_0402_16V6K , SE000000U00) 2.Add PR415(100K_0402_5% , SD028100380)	2015/12/14	DVT
18	Add RF solution for CPU CORE	38	PR803 & PR829 change from 0 ohm to 2.2 0hm	2015/12/14	DVT
19	Change APU_CORE output capacitor	39	PC1084 change from 470U_X_2VY_R9M to 330U_D3_2.5VY_R6M(SGA00006A00)	2015/12/14	DVT
20	Add RF solution		Add PC432 , PC838 , PC839 , PC1088(22P_0402_50V8J,SE068220K80)	2015/12/14	DVT

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				Rev 0.1	

Item	Reason for change	PG#	Modify List	Date	Phase
1	Modify footprint for QFN IC		Modify PU301,PU401,PU402,PU501,PU701,PU801,PU1401,PU1402 footprint	2015/12/16	DVT
2	ADD RF solution	38	Add PC840(22P_0402_50V8J,SE068220K80)	2015/12/16	DVT
3	To reduce 0-ohm part count		Change PR304,PR305 ,PR336,PR322,PR821,PR1410 to 0-ohm short pad	2015/12/16	DVT
4	Delete EVT reserve 0-ohm part		Delete PR823 & PR1408(EVT reserve only)	2015/12/16	DVT

Page 1 of 1
for HW

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				Size	Document Number	Rev	
				Custym		0.2	
				Date:	Thursday, December 17, 2015	Sheet	43 of 43